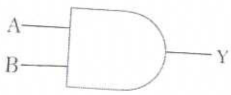
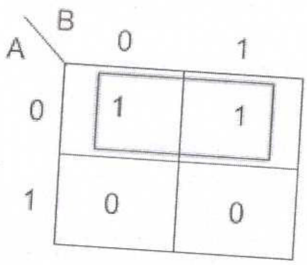
A

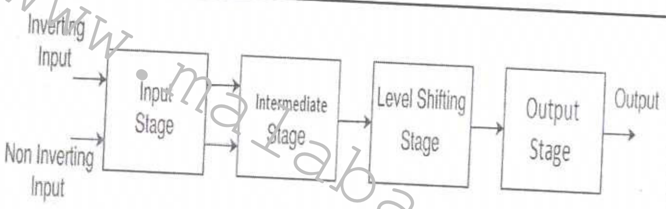
Scoring Indicators

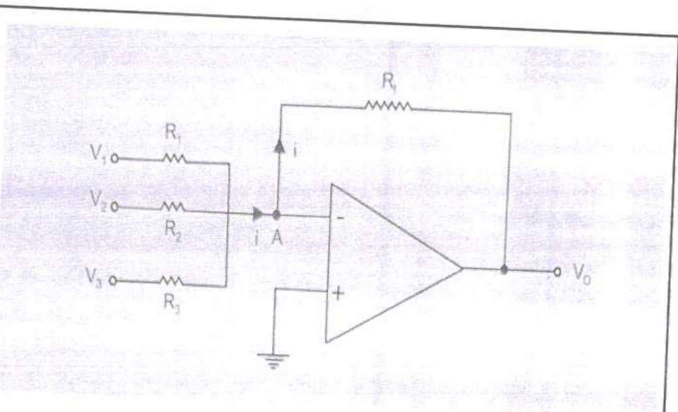
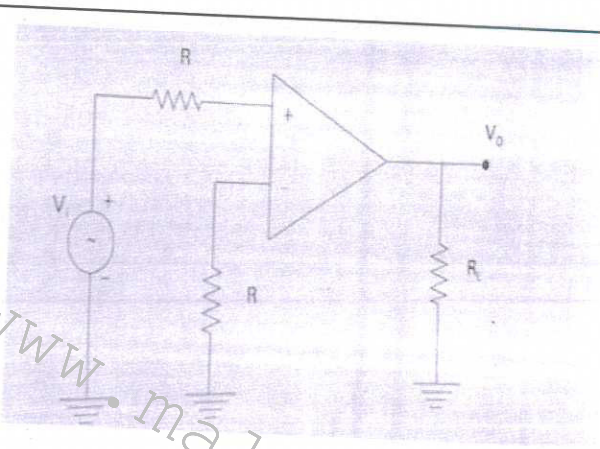
COURSE NAME : ANALOG AND DIGITAL CIRCUITS

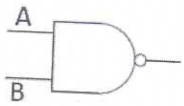
COURSE CODE : 3031

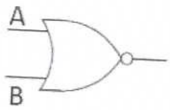
QID:2110220131

Q No	Scoring Indicators	Split score	Sub Total	Total Score
	PART A			
I.1.	*Any two* Direct coupling ,RC coupling, transformer coupling	2x0.5	1	9
I. 2.	Positive feedback	1	1	
I. 3.	Common Mode Rejection Ratio (CMRR) of an opamp is defined as the ratio of the differential voltage gain to the common mode voltage gain.	1	1	
I. 4.	To rectify the input voltage of a very small magnitude, even less than the forward voltage drop of the diode.	1	1	
I. 5.	2's complement of 10110 = 01010	1	1	
I. 6.		1	1	
I. 7.	 Reduced expression for function F= $\overline{A}$		1	

<table>
<tr><td>I. 8.</td><td><table>
<tr><td colspan="2">Input</td><td colspan="2">Output</td></tr>
<tr><td>A</td><td>B</td><td>Sum</td><td>Carry</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td></tr>
</table></td><td></td><td>1</td><td></td></tr>
<tr><td>I. 9.</td><td>2</td><td></td><td>1</td><td></td></tr>
<tr><td></td><td>PART B</td><td></td><td></td><td>24</td></tr>
<tr><td>II. 1.</td><td>To transfer ac output of one stage to the next stage input
To isolate the dc conditions of one stage from the next stage
To eliminate the loaded effect of one stage on the previous stage</td><td>3x1</td><td>3</td><td></td></tr>
<tr><td>II. 2.</td><td>
</td><td>-</td><td>3</td><td></td></tr>
<tr><td>II. 3.</td><td>Any 3 characteristics</td><td>3x1</td><td>3</td><td></td></tr>
<tr><td></td><td>Infinite Input resistance
Zero Output resistance
Infinite voltage gain
Infinite bandwidth
Infinite CMRR
Infinite Slew rate</td><td></td><td></td><td></td></tr>
</table>

<table>
<tr><td>II.4</td><td>
</td><td></td><td>3</td><td></td></tr>
<tr><td>II.5.</td><td>
</td><td></td><td>3</td><td></td></tr>
<tr><td>II.6.</td><td>Division of 1001110 by 100 = 10011.1</td><td></td><td>3</td><td></td></tr>
<tr><td>II.7.</td><td>Listing- 0.5 mark each
Symbol– 0.5 mark each
Truth table-0.5 marks each

Universal gates- NAND ,NOR


NAND
<table><tr><th>A</th><th>B</th><th>Output</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>


NOR
<table><tr><th>A</th><th>B</th><th>Output</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table></td><td>1+1+1</td><td>3</td><td></td></tr>
<tr><td>II.8.</td><td>$Y= \overline{(\bar{A} + B) + CD} = \overline{(\bar{A} + B)}\,\overline{CD} = \bar{\bar{A}}\,\bar{B}\,(\bar{C} + \bar{D})$
$Y = A\bar{B}\,\bar{C} + A\bar{B}\,\bar{D}$</td><td></td><td>3</td><td></td></tr>
</table>

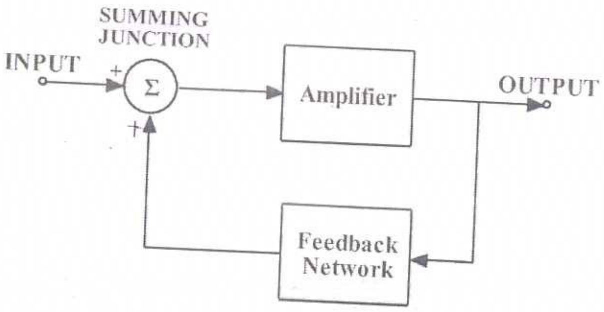
II.9.	f(A,B,C) = $AB + AC + BC$ $= AB(C+\overline{C}) + AC(B+\overline{B}) + BC(A+\overline{A})$ $= ABC + AB\overline{C} + ACB + AC\overline{B} + BCA + BC\overline{A}$ Standard SOP form is $f(A,B,C) = ABC + AB\overline{C} + AC\overline{B} + BC\overline{A}$		3	
II.10.	***Any 3 applications***	3x1	3	
	• Parallel data storage • Serial data storage • Transfer of data • Serial to parallel conversion • Parallel to serial conversion • Counting • Frequency division			
	PART C			42
III	***Any 4 comparisons***		7	
IV	***Block diagram - 3 marks***		7	

Table for III:

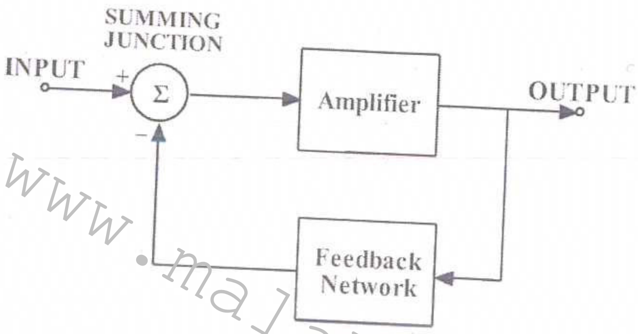
	Class A	Class B	Class C
Transistor is on for	One full cycle	Half cycle	Less than a half cycle
Operating point	Middle of load line	Set at cut off point	Set at below cut off point
Max efficiency	50%	78.5%	85-90%
Output	No distortion	Distorted output	Heavily distorted output

Any 4 differences - 4 marks

Positive feedback

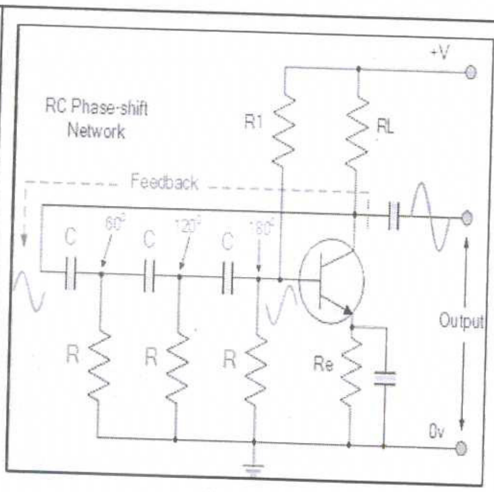


Negative feedback

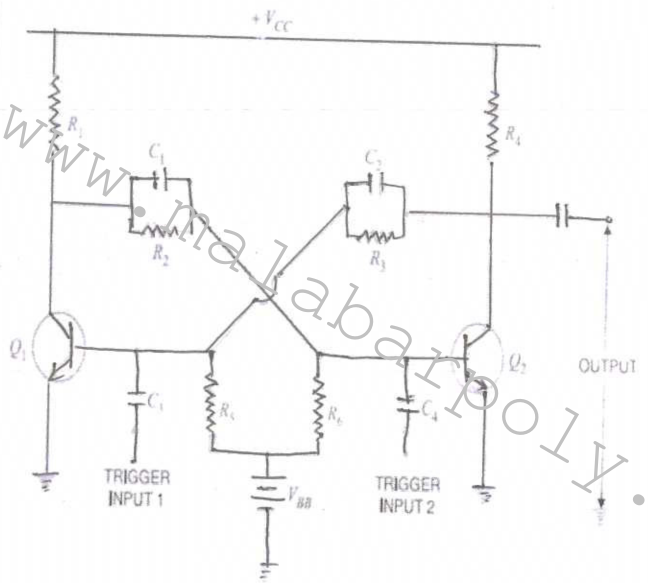


Positive feedback	Negative feedback
The feedback signal is in phase with the input signal	The feedback signal is 180 degree out of phase with the input signal
It increases the gain of the amplifier	It decreases the gain of the amplifier
It increases the noise & distortion	It decreases the noise & distortion
It decreases the stability of amplifier gain	It increases the stability of amplifier gain

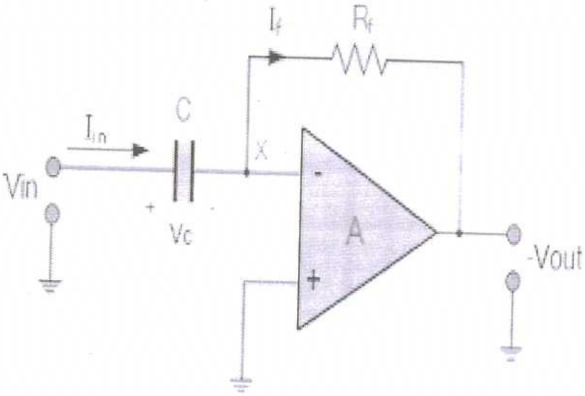
V	*Diagram-4 marks* *Working-3 marks*	4+3	7	

	 The CE amplifier provides 180 degree phase shift.Therefore,to satisfy Barkhausen's criteria ,the feedback circuit must provide 180 degree phase shift.Hence the phase shift feedback network consists of 3 RC sections.Each RC section provides a phase shift of 60°. Thus a total 60° x 3 =180° phase shift is provided by RC phase shift feedback network.The value of resistors and capacitors of RC network and amplifiers are so chosen such that it satisfies Barkhausen Criterion.Frequency of oscillations $f_o=1/(2\pi RC\sqrt{6})$			
VI	***Diagram-4 marks*** ***Explanation-3 marks***	4+3	7	
	Bistable multivibrator has two stable states.It can stay in one of its two states indefinitely (as long as power is supplied)changing to the other state only when it receives a trigger pulse from outside. When Vcc is applied,one transistor will start conducting due to differences in the characteristics of the transistors.If Q1 starts conducting,it is driven to saturation & Q2 is driven to cut off.The circuit will remain in this condition till a trigger pulse is applied.			

	When a negative trigger pulse is applied to the base of Q1 through C3,the forward bias on Q1 will reduce.This decreases the collector current and increases collector voltage.The rising collector voltage is coupled to the base of Q2.BE junction of Q2 is forward biased. This increases the collector current of Q2 and reduces collector voltage.The decreasing voltage is applied to the base of Q1 and it further reverse biases BE junction of Q1.Thus Q1 is driven to cut off and Q2 is driven to saturation . The circuit remains stable at this state until a negative trigger pulse is applied to Q2.			



VII	***Diagram - 4 marks*** ***Derivation- 3 marks***	4+3	7	



Referring to fig, Opamp draws no current(i=0), all current flowing through C must flow through R_f. That is

$$I_{in}=I_f$$

$$C\frac{d}{dt}(V_{in} - V_-) \quad = (V_- - V_{out})/R_f$$

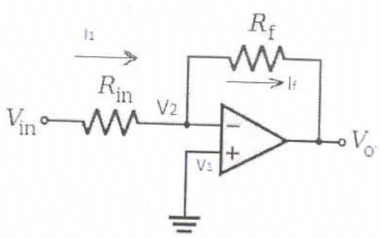
But $V_+=V_- =0$ (Virtual ground).

$$C\frac{d}{dt}(V_{in}) = -V_{out}/R_f$$

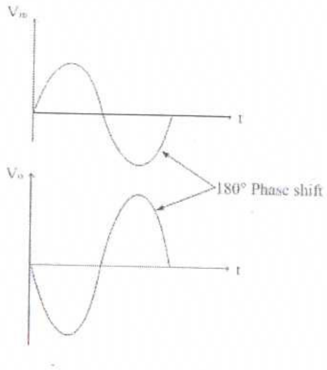
Hence the output voltage of differentiator is

$$V_{out} = -CR_f \frac{d}{dt}(V_{in})$$

VIII	***Circuit diagram-4 marks*** ***Explanation-3marks***	4+3	7	



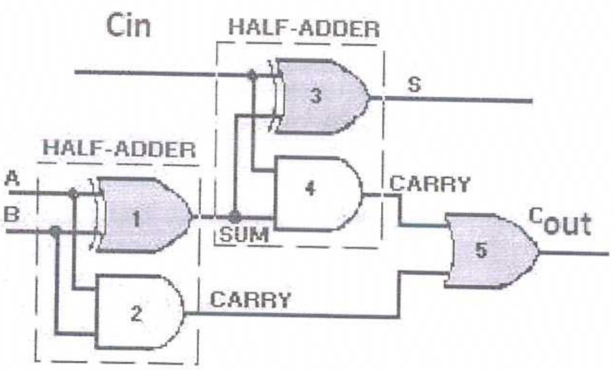
An amplifier whose output voltage is out of phase by 180 degree with respect to the input voltage is known as an inverting amplifier.The input signal Vin is applied to the inverting input terminal through Rin.Non inverting

<table>
<tr><td></td><td>input terminal of opamp is connected to ground. R_f is called feedback resistor. The output voltage Vout is fed back to the inverting terminal through the resistor R_f.

Gain A=Vo/Vin =-Rf/Rin</td><td></td><td></td><td></td></tr>
<tr><td>IX</td><td>Conversion into decimal - 1.5 marks each
Hexadecimal-2 marks each</td><td>3
4</td><td>7</td><td></td></tr>
<tr><td></td><td>a) 1101.101
Equivalent Decimal number $=(13.625)_{10}$
Equivalent Hexadecimal number $=(D.A)_{16}$
b) 10010.01
Equivalent Decimal number $=(18.25)_{10}$
Equivalent Hexadecimal number $=(12.4)_{16}$</td><td></td><td></td><td></td></tr>
<tr><td>X</td><td>Kmap - 4 Marks
Simplification - 3 marks</td><td>4+3</td><td>7</td><td></td></tr>
<tr><td></td><td><table><tr><td>A,B \ C</td><td>0</td><td>1</td></tr><tr><td>00</td><td>1</td><td>0</td></tr><tr><td>01</td><td>1</td><td>1</td></tr><tr><td>11</td><td>1</td><td>0</td></tr><tr><td>10</td><td>1</td><td>1</td></tr></table>
$Y=\overline{C}+\overline{A}B+A\overline{B}$</td><td></td><td></td><td></td></tr>
</table>

XI

Diagram - 4 marks
Truth table - 1 marks
Explanation -2 marks

4 1 2 — 7



A	B	Cin	S	Cout
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

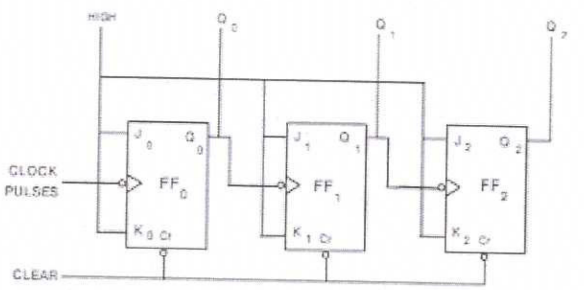
S = $A \oplus B \oplus Cin$

Cout = $(A \oplus B)Cin + AB$

XII

Diagram- 4 marks
Explanation - 3 marks

3+4 — 7



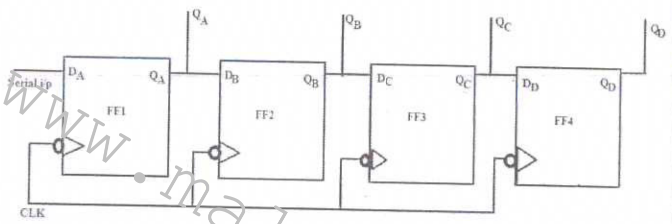
Three flip flops are used to count 8 values.High value is given to J & K so that flip flop will toggle at the application of each clock pulse.Output of a flip flop is

	connected to the clock of the next flip flop. Qo is LSB and Q2 is MSB.			

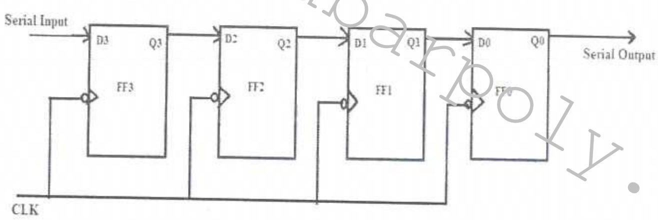
Counter state	Q2	Q1	Q0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

XIII	***Logic diagram -3.5 marks each***	3.5x2	7	

SIPO

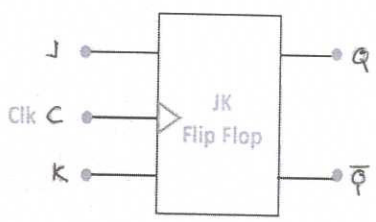


SISO



XIV	***Symbol -1.5 marks each*** ***Truth table -2 marks each***	3+4	7	

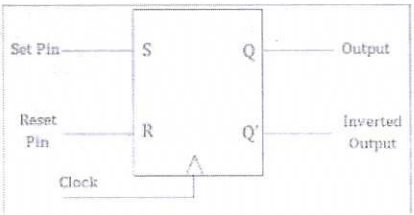
JK FLIP FLOP



Clk	J	K	Q	Q'	State
1	0	0	Q	Q'	No change in state
1	0	1	0	1	Resets Q to 0
1	1	0	1	0	Sets Q to 1
1	1	1	-	-	Toggles

Truth table

SR FLIP FLOP



INPUTS			OUTPUT	STATE
CLK	S	R	Q	
X	0	0	No Change	Previous
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	-	Forbidden

Truth table

Remya
15/11/22
Remya Mohanan
Lecturer in EEE