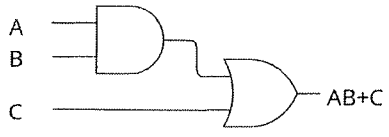
Set : 2

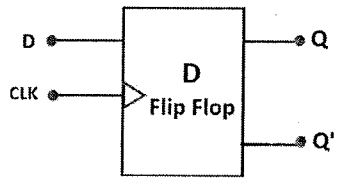
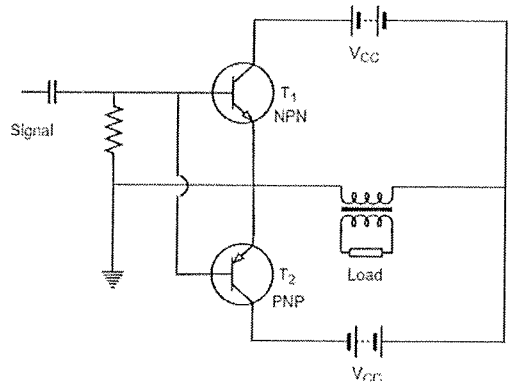
QID : 2110220128

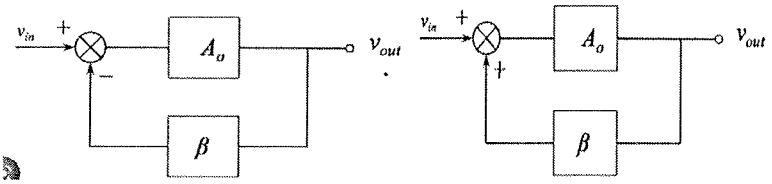
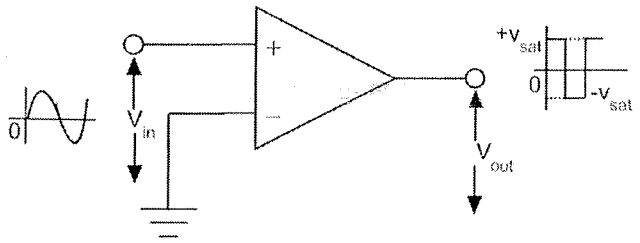
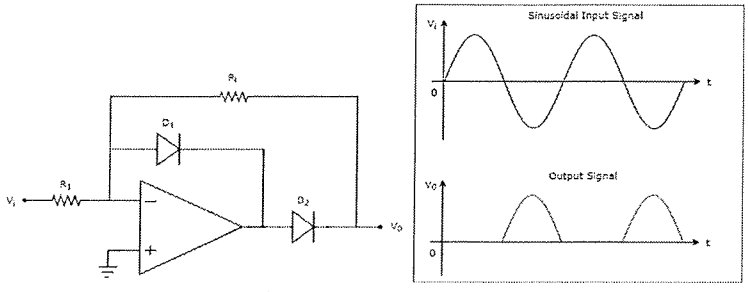
Scoring Indicators

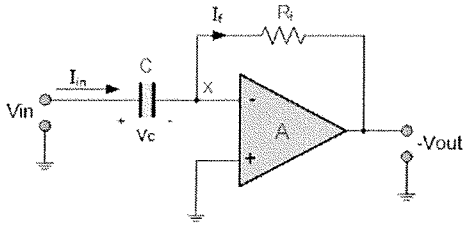
Paper II

3031 **ANALOG & DIGITAL CIRCUITS**

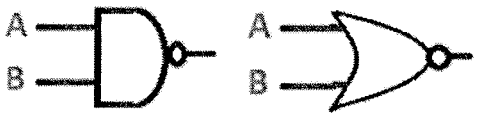
Q No	Scoring Indicators	Split score	Sub Total	Total score
	PART A			
I. 1	Negative feedback	1	1	1
I. 2	The oscillator is used in Watches. Oscillators are used in Radio Circuits Oscillators are used smartphones, computer laptops etc. **Answer any 2**	0.5*2	1	1
I. 3	The ratio of the differential-mode to common-mode gain is called CMRR	1	1	1
I. 4	Inverting amplifier Output voltage=(-Rf/Rin) Vin	0.5*2	1	1
I. 5	1. $\overline{(A + B)} = \overline{A}.\ \overline{B}$ 2. $\overline{(A.B)} = \overline{A} + \overline{B}$	0.5*2	1	1
I. 6	1010 0010 + 1=1010 0011	1	1	1
I. 7		1	1	1
I. 8	Frequency dividers. Counters. Storage registers. Shift registers **Answer any two**	0.5*2	1	1

I. 9		1	1	1
	PART B			
II. 1	 The above circuit employs a NPN transistor and a PNP transistor connected in push pull configuration. When the input signal is applied, during the positive half cycle of the input signal, the NPN transistor conducts and the PNP transistor cuts off. During the negative half cycle, the NPN transistor cuts off and the PNP transistor conducts	2 1	3	3
II. 2	**Coupling schemes:** Transformer coupling, RC coupling and Direct coupling **Need for coupling(Answer any 2)** 1. To transfer ac output of one stage to the next stage input 2. To isolate the dc conditions of one stage from the next stage 3. To minimize loading effect	1 2	3	3
II. 3	1. The output current flows for the entire cycle of the AC input supply 2. Conduction angle is 360 degree 3. Q point is placed at the midpoint of dc load line 4. No distortion is present **Answer any three**	1*3	3	3

II. 4		1.5*2	3	3
II. 5	1. Input resistance infinity 2. output resistance zero 3. Open loop voltage gain infinity 4. Bandwidth infinity 5. Slew rate infinity 6. CMRR infinity **Answer any three**	1*3	3	3
II. 6	 When the input signal is above ground level, the output of the circuit is saturated at its positive extreme. When the input goes below ground level, the output voltage of the circuit immediately switches to its negative saturation level. Every time when the input signal crosses the zero voltage level, the output switches between one saturation level and the other	2 1	3	3
II. 7		1.5*2	3	3

<table>
<tr>
<td>II. 8</td>
<td> 

V_{out}= -$R_f C \frac{d}{dt}(Vin)$</td>
<td>2

1</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>II. 9</td>
<td> 

<table>
<tr><th>A</th><th>B</th><th>NAND</th><th>NOR</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td></tr>
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<td>1

2</td>
<td>3</td>
<td>3</td>
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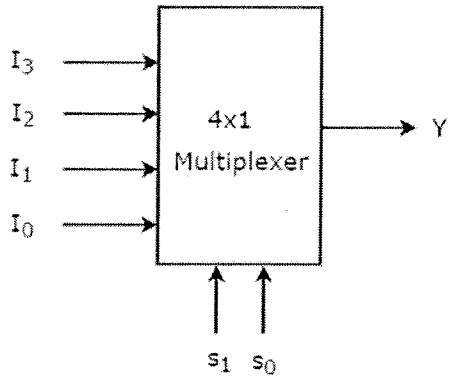
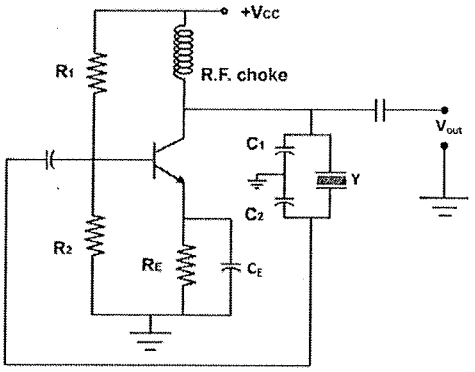
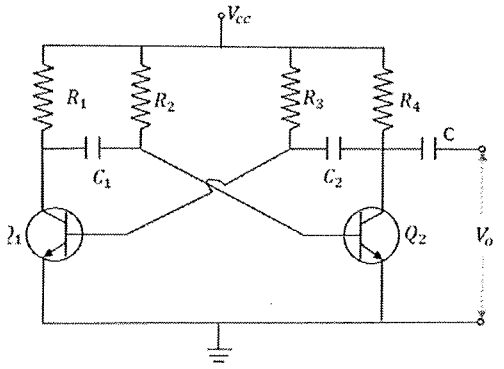
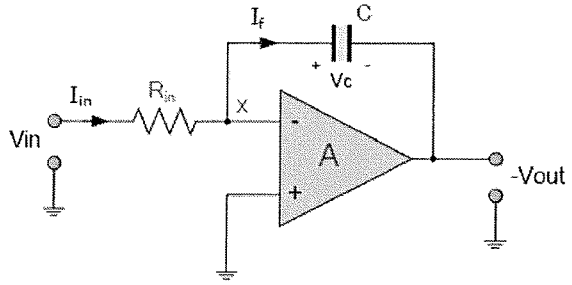
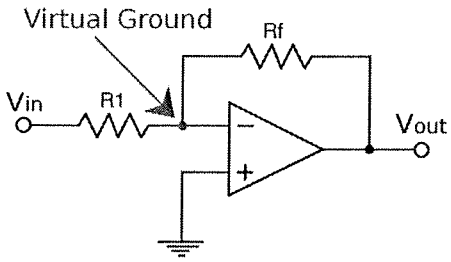
<tr>
<td>II.10</td>
<td> 

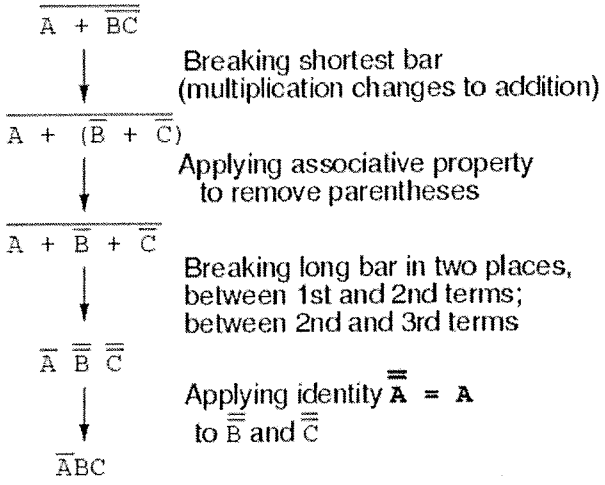
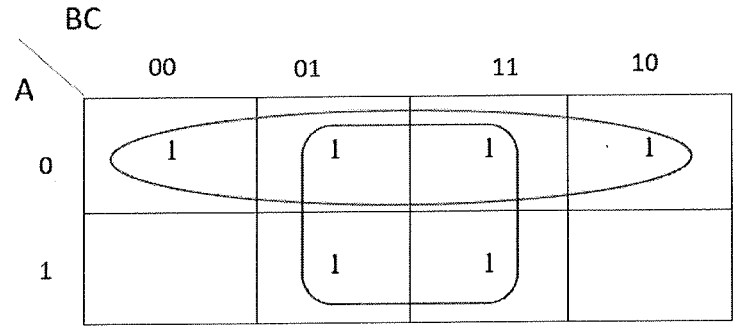
<table>
<tr><th>S_1</th><th>S_0</th><th>Y</th></tr>
<tr><td>0</td><td>0</td><td>I_0</td></tr>
<tr><td>0</td><td>1</td><td>I_1</td></tr>
<tr><td>1</td><td>0</td><td>I_2</td></tr>
</table></td>
<td>1

2</td>
<td>3</td>
<td>3</td>
</tr>
</table>

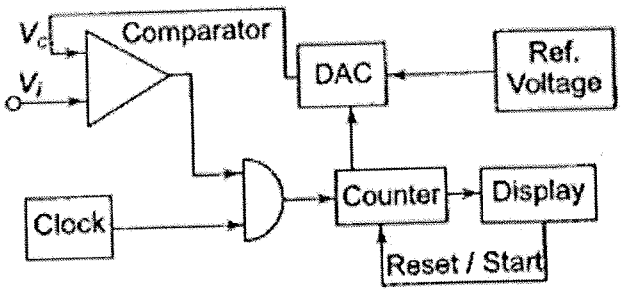
		1	1	I3	
	PART C				
III	 The crystal will act as a parallel-tuned circuit. As we can see in this circuit that instead of resonance caused by L and (C1+C2), we have the parallel resonance of the crystal. At parallel resonance, the impedance of the crystal is maximum. This means that there is a maximum voltage drop across C1. This in turn will allow the maximum energy transfer through the feedback network at the parallel resonant frequency *fp* which is given by: $f_p = \frac{1}{2\pi\sqrt{L}C_T}$ Where, $C_T = \frac{C \times C_m}{C + C_m}$ Note that feedback is positive. A phase shift of is produced by the transistor. A further phase shift of is produced by the capacitor voltage divider. This oscillator will oscillate only at *fp* . Even a small deviation from *fp* will cause the oscillator to act as an effective short. Consequently, we have an extremely stable oscillator.	4 3	7	7

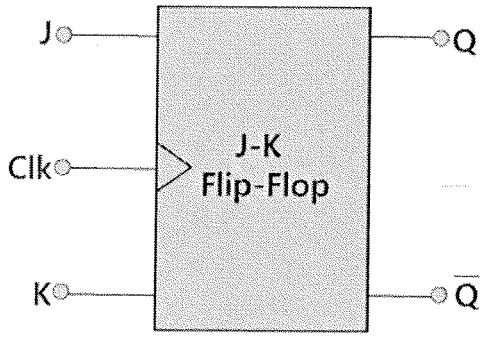
IV	 As no transistor characteristics are alike, one of the two transistors say Q1 has its collector current increase and thus conducts. The collector of Q1 is applied to the base of Q2 through C1. This connection lets the increased negative voltage at the collector of Q1 to get applied at the base of Q2 and its collector current decreases. This continuous action makes the collector current of Q2 to decrease further. This current when applied to the base of Q1 makes it more negative and with the cumulative actions Q1 gets into saturation and Q2 to cut off. Thus the output voltage of Q1 will be VCE (sat) and Q2 will be equal to VCC. The capacitor C1 charges through R1 and when the voltage across C1 reaches 0.7v, this is enough to turn the transistor Q2 to saturation. As this voltage is applied to the base of Q2, it gets into saturation, decreasing its collector current. This reduction of voltage at point B is applied to the base of transistor Q1 through C2 which makes the Q1 reverse bias. A series of these actions turn the transistor Q1 to cut off and transistor Q2 to saturation. Now point A has the potential VCC. The capacitor C2 charges through R2. The voltage across this capacitor C2 when gets to 0.7v, turns on the transistor Q1 to saturation.	4 3	7	7

V	 $I_{in} = I_f$ $\frac{(Vin-x)}{Rin} = C.\frac{d(x-V0)}{dt}$;x=0 $\frac{Vin}{Rin} = C.\frac{-d(V0)}{dt}$ $dV0 = \frac{-1}{Rin.C}(Vin.dt)$ Integrating both sides we get $V0 = \frac{-1}{Rin.C}\int Vin\ dt$	4 3		
VI	 A virtual ground is a node of a circuit that is at a steady reference potential, without being directly connected to the reference potential. It is a concept that is made for easy explanation and calculation purposes as voltage is approximately zero. In the above circuit, as the value of gain is infinity , the differential input to the op amp is zero. Since the voltage at non inverting terminal is zero, voltage at inverting terminal is also equal to zero	3 4	7	7

VII	a. $\overline{A.(A+C)} = \overline{A} + \overline{(A+C)}$ ie=$\overline{A} + (\overline{A}.\overline{C})$ =$\overline{A}(1+\overline{C})$ =$\overline{A}$ b.  	3 4	7	7
VIII	$(1\ 1100\ 1011.\ 101)_2$ $=(1 \times 2^8) + (1 \times 2^7) + (1 \times 2^6) + (0 \times 2^5) + (0 \times 2^4) + (1 \times 2^3) + (0 \times 2^2) + (1 \times 2^1) + (1 \times 2^0) + (1 \times 2^{-1}) + (0 \times 2^{-2}) + (1 \times 2^{-3}) = (459.625)_{10}$	7	7	7
IX	Structure of K map Mapping value Grouping Final result f(A,B,C)= Σm(0,1,2,3,5,7)  Y= $\overline{A}$+C	2 1 2 2	7	7

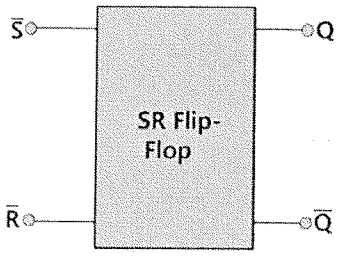
X	a. $$\begin{array}{r} 11011 \\ \times \quad 101 \\ \hline 11011 \\ 00000 \\ + \ 11011 \\ \hline 10000111 \end{array}$$ b. **111010 ÷ 100 = 1110.1** $$\begin{array}{r} 1110.1 \\ 100 \overline{)\,111010.0} \\ -100 \\ \hline 110 \\ -100 \\ \hline 101 \\ -100 \\ \hline 100 \\ -100 \\ \hline 0 \end{array}$$	3 4	7	7
XI	<table><tr><th>Synchronous</th><th>Asynchromous</th></tr><tr><td>Synchronous Counter is faster than asynchronous counter in operation</td><td>Asynchronous Counter is slower than synchronous counter in operation</td></tr><tr><td>In synchronous counter, all flip flops are triggered with same clock simultaneously</td><td>In asynchronous counter, different flip flops are triggered with different clock, not simultaneously</td></tr><tr><td>Synchronous Counter does not produce any decoding errors</td><td>Asynchronous Counter produces decoding error</td></tr></table>		7	7

	Synchronous Counter is also called Parallel Counter	Asynchronous Counter is also called Serial Counter		
	Synchronous Counter designing as well implementation are complex due to increasing the number of states	Asynchronous Counter designing as well as implementation is very easy		
	Synchronous Counter will operate in any desired count sequence.	Asynchronous Counter will operate only in fixed count sequence (UP/DOWN)		
	Synchronous Counter examples are: Ring counter, Johnson counter	Asynchronous Counter examples are: Ripple UP counter, Ripple DOWN counter		
	In synchronous counter, propagation delay is less	In asynchronous counter, there is high propagation delay		
XII	 Two inputs are applied to the comparator in the figure above. These are: (1) the analog input, and (2) a linear ramp (sawtooth) voltage from the ramp generator. The generator output is initiated each time a start signal is applied. The start signal also resets the counter to zero and enables the gate circuit.As long as the analog and ramp generator inputs to the comparator differ in magnitude, the clock pulse generator will be permitted to transmit pulses at a constant repetition rate through the gate into the counter. When the two inputs to the comparator become equal (as a result of the linearly rising	4 3	7	7

	sawtooth) the comparator will generate a stop signal which disables the gate circuit and ends the comparison time interval. The disabled gate circuit blocks the flow of pulses from the clock pulse generator to the counter. The number of pulses accumulated in the counter during the comparison time interval is proportional to the amplitude of the analog input voltage.			
XIII	a.  Symbol		7	7

J	K	Q	Qn+1	Remarks
0	0	0	0	No change
0	1	0	0	Reset
1	0	0	1	Set
1	1	0	1	Toggle
0	0	1	1	No change
0	1	1	0	Reset
1	0	1	1	Set
1	1	1	0	Toggle

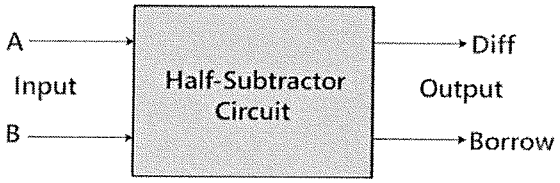
b.



Symbol

S	R	Q	Qn+1	Remarks
0	0	1	1	Invalid
0	1	0	0	Reset
1	0	0	1	Set
1	1	0	0	No change
0	0	1	1	Invalid
0	1	1	0	Reset
1	0	1	1	Set
1	1	1	1	No change

XIV



Inputs		Outputs	
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Diff= $\overline{A}$B + A$\overline{B}$ = A⊕B

Borrow = $\overline{A}$ B

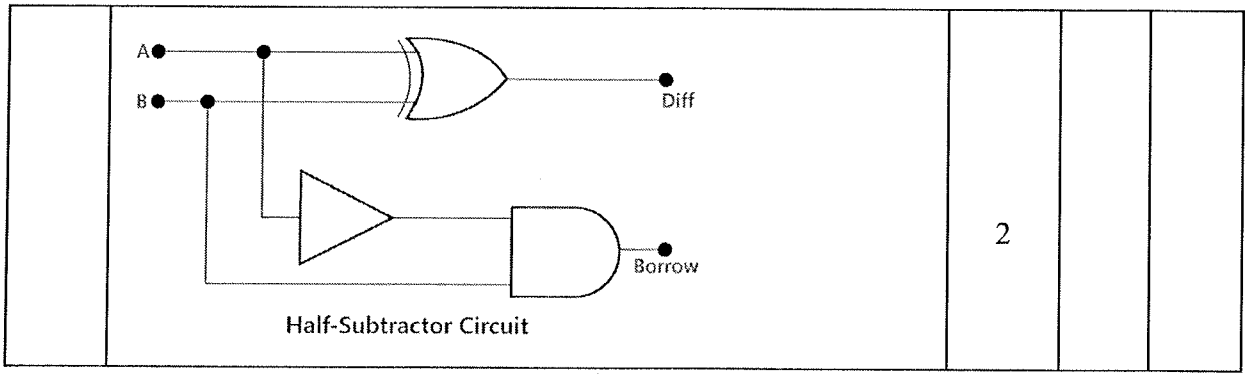
1

2

2

7

7


A
B
Diff
Borrow
Half-Subtractor Circuit
2