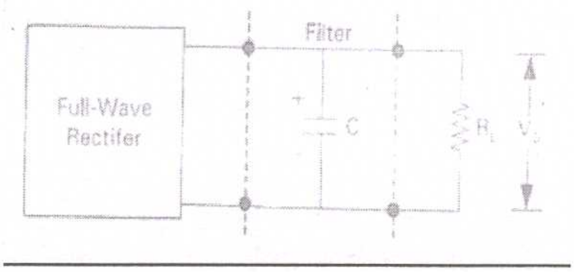
35 D (1) April-24 Page No - 18

CODE - 3031

Course Title: ANALOG DEVICES AND CIRCUITS			
Qst.No.	Scoring Indicator	Split up	Total
	PART A		
1	Peak inverse voltage may be defined as the maximum voltage that can be with stand by a diode in reverse biased conditions	2	2
2	• Negative feedback reduces noise and distortion • It improves stability of amplifier gain • It increases the bandwidth • It increases input impedance Any two of the above	1x2	2
3	The Barkhausen criterion states that: The loop gain is equal to unity in absolute magnitude, that is, $\mid \beta A \mid = 1$ and the phase shift around the loop is zero or an integer multiple of 2π radian (180°)	1×2	2
4	CMMR stands for Common Mode Rejection Ratio and it is defined as the ratio of differential voltage gain to common mode voltage gain CMMR =Ad/Ac	1×2	2
5	Av = -Rf/R1 Where: Av is the voltage gain Rf is the feedback resistor R1 is the input resistor	2	2
	PART B		
1	Shunt capacitor filter: Diagram 	2 2	6

1

	Waveforms  Explanation The capacitance offers a low reactance path to the ac component of current. During the positive half cycle, the capacitor charges to the peak voltage Vm. Just past the positive peak, the rectifier output voltage tries to fall. But at point B. the capacitor has +Vm voltage across it. Since the source voltage becomes slightly less than Vm, the diode is reverse biased and becomes open circuited. The diode disconnects the source from the load. The capacitor starts to discharge through the load. This prevents the load voltage from falling to zero. The capacitor continues to discharge until the source voltage becomes more than the capacitor voltage (at point C). The diode again starts conducting, the capacitor is again charged to peak value Vm. During the time the capacitor is charging (from point C to D) the rectifier supplies the charging current. The current is maintained through the load all the time.	2	

Q	Answer	Marks	Total
2	**Voltage regulator using 7805 IC**	3	6

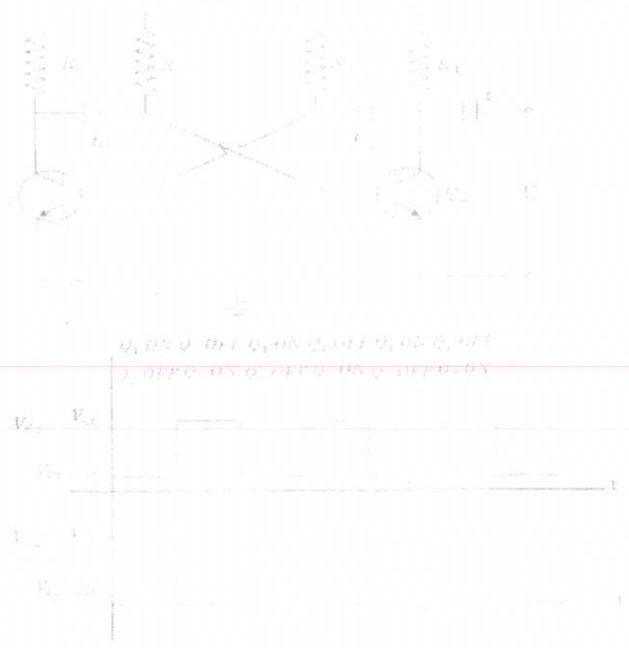
Diagram

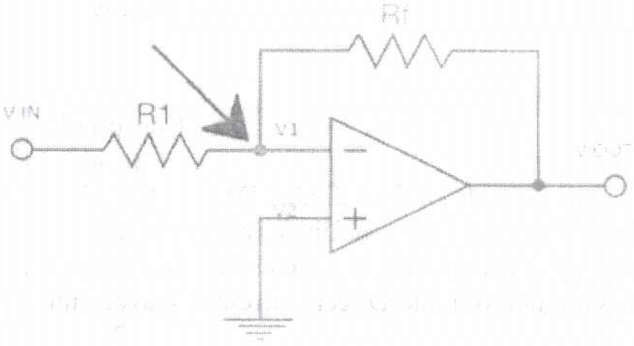
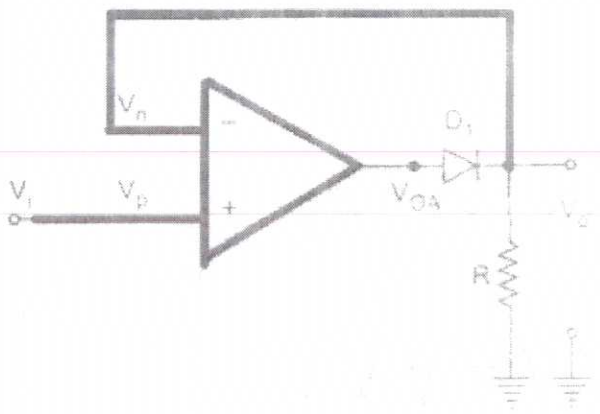
Explanation

Pin 1 is the input terminal pin 2 the ground and pin 3 is 3 the output terminal. The unregulated input voltage (Vi) is given to the input terminal. The output is taken from the output terminal. Filter capacitors are shown to be connected at the input and output side. The input capacitor C1 is used to cancel the inductive effects due to long distribution leads and the output capacitor C, improves the transient response — 3

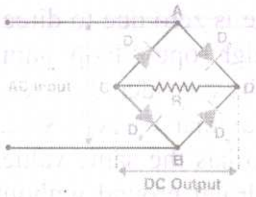
Q	Answer	Marks	Total
3		1x6	6

POSITIVE	NEGATIVE
Feedback signal is in same phase	Feedback signal is in phase opposition or 180
Regenerative	Degenerative
Increases Gain	Reduces Gain
Increases the noise	Reduces the noise.
Decreases the stability	Increases stability
Oscillators	Amplifiers

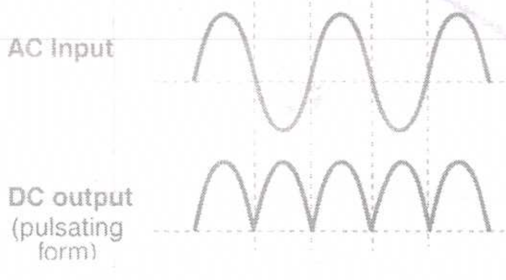
4	Explanation: In many electronic systems the final output is in the form of sound. In such systems, the final stage has to be a power amplifier and the loudspeaker is the load for the power amplifier. The power amplifier drives the loudspeaker. The maximum power will be transferred to the loudspeaker from the power amplifier, <u>only if the power amplifier output impedance is the same as the impedance of the loudspeaker.</u> If it is not so, the loudspeaker gets less power, though the amplifier is capable of delivering more power. So, it is possible to obtain maximum power output, impedance matching is required between the power amplifier and loudspeaker. This can be achieved by using an impedance matching network that matches the loudspeaker impedance to the output impedance of the power amplifier.	6	6
5		3 3	6

6	 The non inverting terminal voltage is zero due to direct grounding. The OP-Amp has high open loop gain. Therefore, the input current may be considered as zero in approximation. Hence we can say that V1=V2. Since V2 is at ground potential. VI also has the same value, that is zero. Hence it acts as a virtual ground without being connected to ground.	3 3	6
7	This OP-Amp has unity feedback gain since the output is directly connected to the input When a +ve voltage is applied as input. The diode immediately conducts due to high open loop gain and after conducting, the feed comes in exist. Therefore the output is the same as the input. When a negative voltage is applied, the diode is reverse biased and does not conduct.  	3 3	6
	PART C		

<table>
<tr>
<td>III (a)</td>
<td>
<u>Construction</u>

The bridge rectifier circuit is made of four diodes D1, D2, D3, D4, and a load resistor RL. The four diodes are connected in a closed-loop configuration to efficiently convert the alternating current (AC) into Direct Current (DC).
<u>Circuit Daigram</u>


<u>Working</u>
When an AC signal is applied across the bridge rectifier, terminal A becomes positive during the positive half cycle while terminal B becomes negative. This results in diodes D1 and D3 becoming forward biased while D2 and D4 becoming reverse biased.
During the negative half-cycle, terminal B becomes positive while terminal A becomes negative. This causes diodes D2 and D4 to become forward biased and diode D1 and D3 to be reverse biased.

<u>Waveform</u>


</td>
<td>Construction and Circuit diagram (3)
Working (3)
Waveform(2)</td>
<td>8</td>
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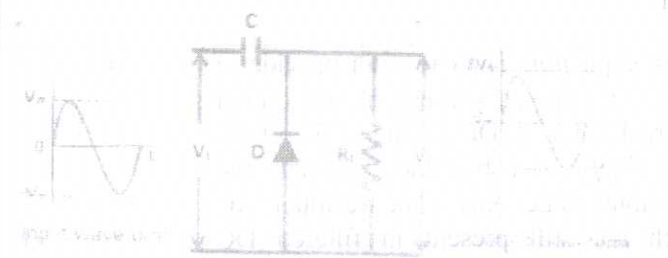
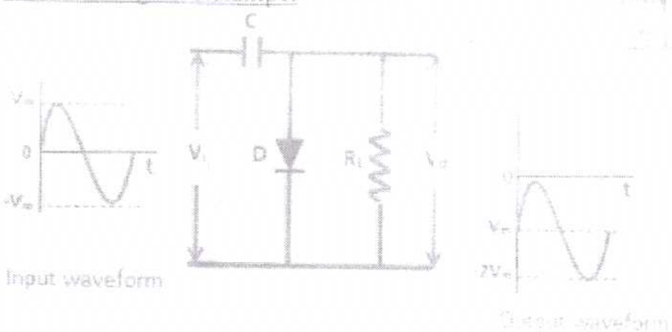
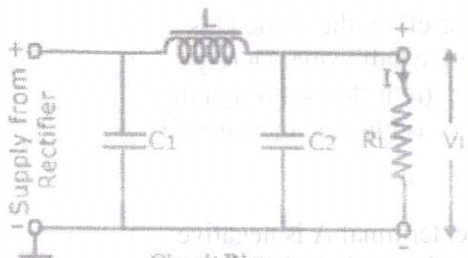
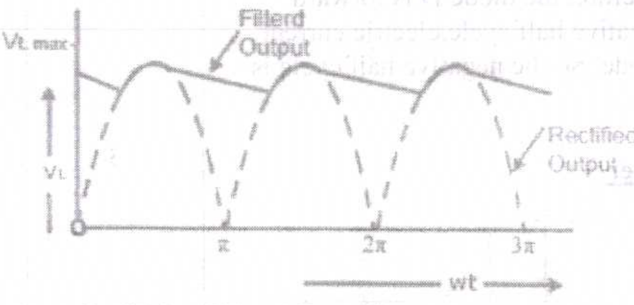
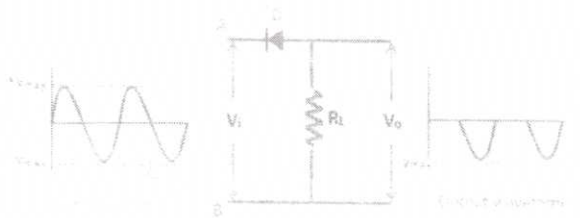
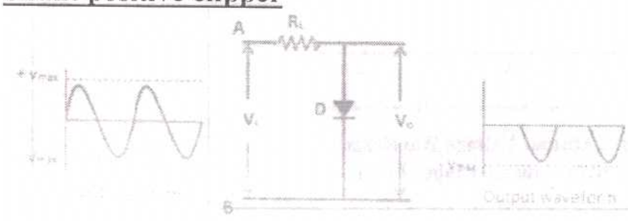
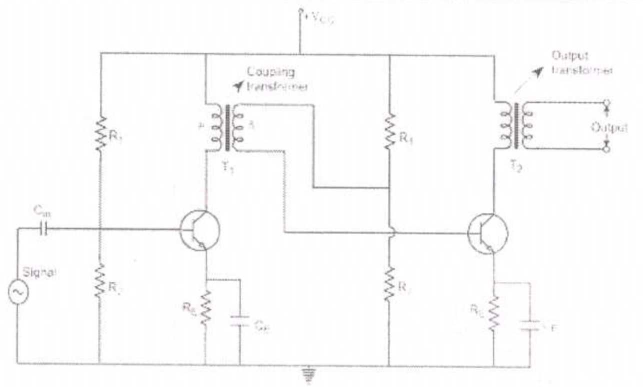
</table>

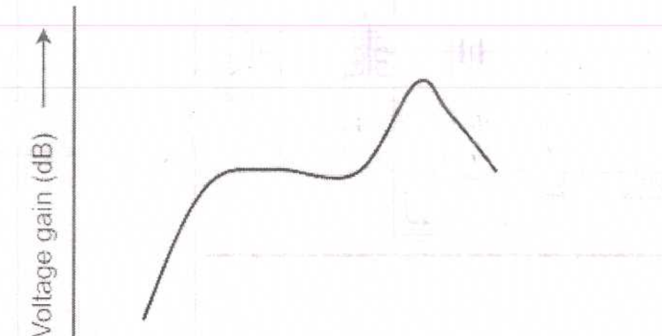
III (b)	unbiased positive clamper  Unbiased negative clamper  Explanation	4 3	7
IV (a)	 **Circuit Diagram**  **Rectified and Filtered Output Voltage Waveform** **Full Wave Rectifier with Capacitor Input Filter** The output voltage coming from the rectifier also consists of AC components. Thus it is a crucial need to remove these AC ripples to improve the performance of the device. The output from the rectifier is directly	4	8

	applied to the input capacitor. The capacitor provides a low impedance to AC ripples present in the output voltage and high resistance to DC voltage. Therefore, most of the AC ripples get bypassed through the capacitor in the input stage only. The residual AC components which are still present in filtered DC signals get filtered when they pass through the inductor coil and through the capacitor connected parallel across the load. In this way, the efficiency of filtering increases multiple times.	4	
IV (b)	**<u>Series positive clipper</u>**  Series positive clipper During the positive hak cycle, terminal A is positive and terminal B is negative. Therefore, the diode D is reverse biased during the positive half cycle. During reverse biased conditions, no current flows through the diode. So the positive half cycle is blocked or removed at the output. During the negative half cycle, terminal A is negative and terminal B is positive then the diode is said to be forward biased. Therefore, the diode D is forward biased during the negative half cycle,electric current flows through the diode. So the negative half cycle is allowed at the output **<u>Shunt positive clipper</u>**  Shunt positive clipper In the shunt positive clipper, during the positive half cycle the diode is forward biased and hence no output is generated. On the other hand, during the negative half cycle the diode is reverse biased and hence the entire negative half cycle appears at the output	4 3	7

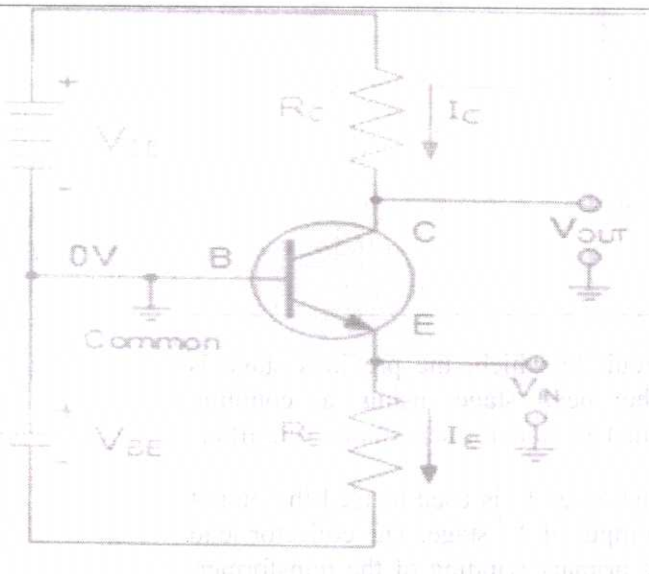
<table>
<tr><td>V(a)</td><td>

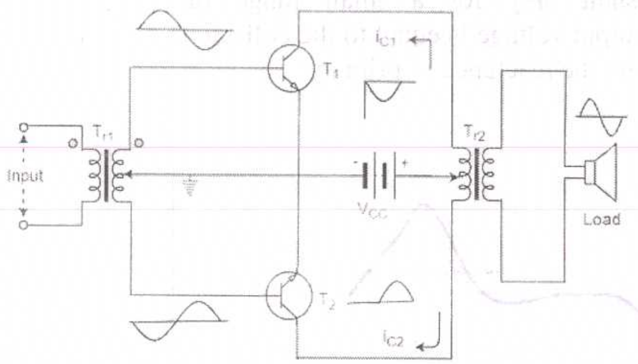


</td><td>4</td><td>8</td></tr>
<tr><td></td><td>The amplifier circuit in which, the previous stage is connected to the next stage using a coupling transformer, is called as Transformer coupled amplifier.</td><td>2</td><td></td></tr>
<tr><td></td><td>The coupling transformer T_1 is used to feed the output of 1^{st} stage to the input of 2^{nd} stage. The collector load is replaced by the primary winding of the transformer. The secondary winding is connected between the potential divider and the base of 2^{nd} stage, which provides the input to the 2^{nd} stage. Instead of coupling capacitor like in RC coupled amplifier, a transformer is used for coupling any two stages, in the transformer coupled amplifier circuit.</td><td></td><td></td></tr>
<tr><td></td><td>The figure below shows the frequency response of a transformer coupled amplifier. The gain of the amplifier is constant only for a small range of frequencies. The output voltage is equal to the collector current multiplied by the reactance of primary.



</td><td>2</td><td></td></tr>
</table>

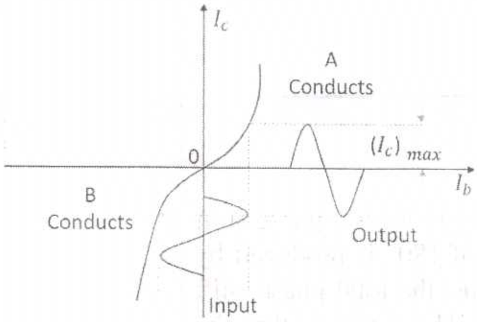
<table>
<tr><td>V(b)</td><td>
</td><td>3</td><td>7</td></tr>
<tr><td></td><td>During the Positive cycle of input, the forward bias of base-emitter junction is decreased because V is negative w.r.t ground resulting in a decrease in Is. The collector current le is also decreased by ß times with the ·decrease in la, hence VCE is correspondingly increased.

Vce=Vcc-IcRc</td><td>4</td><td></td></tr>
<tr><td>VI(a)</td><td>
</td><td>3</td><td>8</td></tr>
<tr><td></td><td><u>Operation</u>

The circuit of the class B push-pull amplifier shown in the above figure clears that both the transformers are center-tapped. When no signal is applied at the input, the transistors T_1 and T_2 are in cut off condition and hence no collector currents flow. As no current is drawn from V_{CC}, no power is wasted.

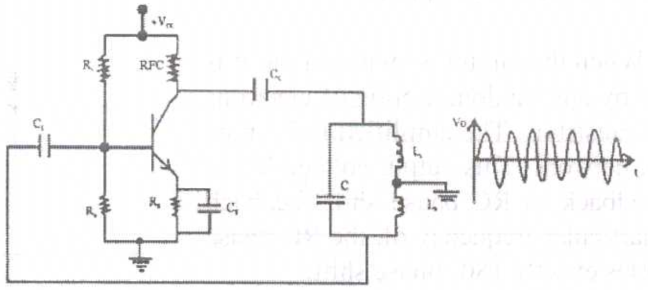
When input signal is given, it is applied to the input transformer T_{r1} which splits the signal into two signals that are 180^{o} out of phase with each other. These two</td><td>4</td><td></td></tr>
</table>

signals are given to the two identical transistors T_1 and T_2. For the positive half cycle, the base of the transistor T_1 becomes positive and collector current flows. At the same time, the transistor T_2 has negative half cycle, which throws the transistor T_2 into cutoff condition and hence no collector current flows. The waveform is produced as shown in the following figure.



1

VI(b)



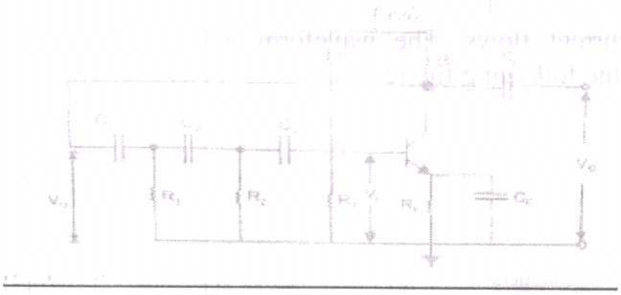
3

Resistors $R_1 R_2$ and R_E provide the required DC bias to the transistor. CC is coupling capacitor and C_E is a bypass capacitor. RFC is radio frequency choke which isolates power supply from the oscillations at the collector. Inductors L_1, L_2 with capacitor C forms the tank circuit. Frequency of oscillations 4

$f = \frac{1}{2\pi\sqrt{LC}}$ Where $L = L_1 + L_2$

When power supply is switched on, collector current increases and charge the capacitor. When the capacitor is fully charged, it discharges through L_1 and L_2 and oscillations will be set up. The voltage across L_2 is feedback to amplifier circuit and that across L_1 is taken as output. 180° phase shift is provided by the transistor amplifier and another 180° phase shift is provided by the tank circuit. Thus totally 360° phase shift is obtained, which is the required condition for the sustained oscillations.

The voltage feedback ratio $\beta = \frac{L_2}{L_1}$

<table>
<tr>
<td>VII(a)</td>
<td>RC phase shift oscillator

<u>Explanation</u>

Since the transistor CE amplifier produces a phase shift of 180° and further phase shift of 180° is produced by the RC phase shift network. Thus, the total phase shift around the entire loop is 360°. The result is that the output of the transistor amplifier is returned to the input in the proper phase to produce oscillations.

Circuit Operation: When the circuit is switched on, it is set into oscillations by any random motion of electrons in elements or the transistor.. The amplified noise now drives the feedback network. This output voltage Vo of the amplifier is feedback to RC phase shift feedback network At some particular frequency of, the RC phase shift network provides exactly 180° phase shift.

The advantages of the RC phase shift oscillator include:(Any two)
• Easy design with basic components like resistors and capacitors
• Low cost
• Excellent frequency stability
• Suitable for low frequencies</td>
<td>3

3

2</td>
<td>8</td>
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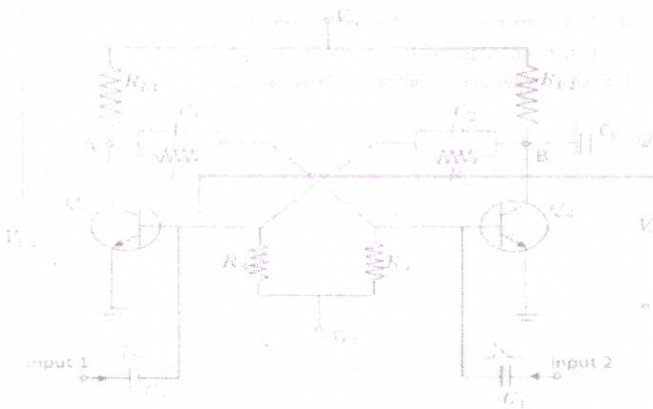
<tr>
<td>VII(b)</td>
<td>

The Bistable Multivibrator is a two state non-regenerative device constructed from two cross-coupled</td>
<td>4

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<td>7</td>
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<table>
<tr>
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<td>transistors operating as "ON-OFF transistor switches. In each of the two states, one of the transistors is cut-off while the other transistor is in saturation, this means that the bistable circuit is capable of remaining indefinitely in either stable state.

To change the bistable over from one state to the other, the bistable circuit requires a suitable trigger pulse and to go through a full cycle two triggering pulses, one for each stage are required. The bistable multivibrator can be switched over from one stable state to the other by the application of an external trigger pulse thus it requires two external trigger pulses before it returns back to its original state</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIII(a)</td>
<td>
<table>
<tr><th>Amplifier</th><th>Oscillator</th></tr>
<tr><td>Amplifier is an electronic circuit which gives output as amplified form of input</td><td>Oscillator is an electronic circuit which gives output without application of input.</td></tr>
<tr><td>The amplifier does not generate any periodic signal</td><td>The oscillator is generating of the periodic electronic signal.</td></tr>
<tr><td>Amplifier uses negative feedback</td><td>Oscillator uses positive feedback</td></tr>
<tr><td>The Amplifier provides amplified signal.</td><td>Oscillator is gives oscillatory signal.</td></tr>
<tr><td>Amplifiers do nothing till input signal is fed to the input</td><td>Oscillators produce signals from the moment of powered</td></tr>
</table>
</td>
<td>For each point 1.5 Mark

For 5 points 8 Mark</td>
<td>8</td>
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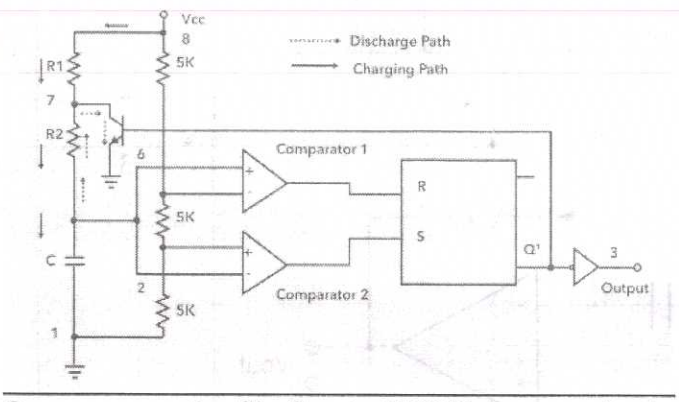
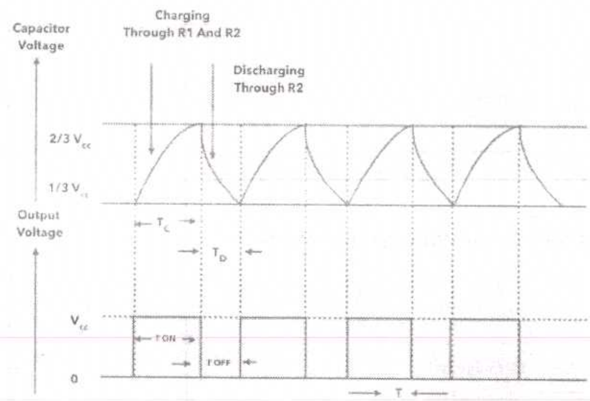
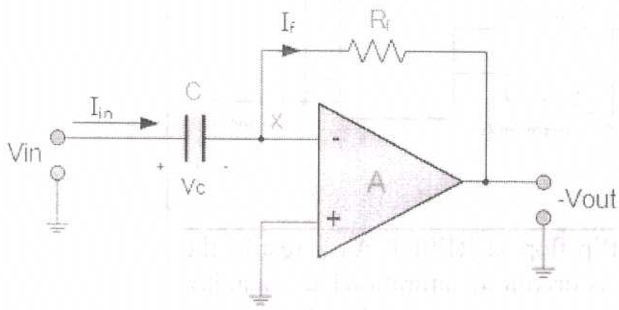
<tr>
<td>VIII(b)</td>
<td>Internal Circuit Of 555 Timer With Astable Mode



On power-up, the flip-flop is RESET As a result, the discharge transistor is driven to saturationThe capacitor C of the timing circuit is connected at Pin 7 of the IC 555 and will discharge through the transistor. The output of the timer at this point is low.The voltage</td>
<td>3

2</td>
<td>7</td>
</tr>
</table>

	across the capacitor is nothing but the trigger voltage. So, while discharging, if the capacitor voltage becomes less than 1/3 VCC, which is the reference voltage to trigger comparator.the output of the comparator 2 will become high. This will SET the flip-flop and hence the output of the timer at pin 3 goes to HIGH.This high output will turn OFF the transistor. As a result, the capacitor C starts charging through the resistors R1 and R2. Now, the capacitor voltage is the same as the threshold voltage. While charging, the capacitor voltage increases exponentially towards VCC and the moment it crosses 2/3 VCC, which is the reference voltage to threshold comparator (comparator 1), its output becomes high.As a result, the flip-flop is RESET. The output of the timer falls to LOW. This low output will once again turn on the transistor which provides a discharge path to the capacitor. Hence the capacitor C will discharge through the resistor R2. And hence the cycle continues. Waveforms Of Capacitor Voltage And Output Voltage 	2	
IX(a)	 The basic operational amplifier differentiator circuit produces an output signal which is the first derivative of the input signal	3 5	8

<table>
<tr><td></td><td>

$$I_{IN} = I_F \text{ and } I_F = \frac{V_{OUT}}{R_F}$$

The charge on the capacitor equals Capacitance times Voltage across the capacitor

$$Q = C \times V_{IN}$$

Thus the rate of change of this charge is:

$$\frac{dQ}{dt} = C\frac{dV_{IN}}{dt}$$

but dQ/dt is the capacitor current, *i*

$$I_{IN} = C\frac{dV_{IN}}{dt} = I_F$$

$$\therefore \frac{V_{OUT}}{R_F} = C\frac{dV_{IN}}{dt}$$

From which we have an ideal voltage output for the op-amp differentiator is given as:

$$V_{OUT} = -R_F C\frac{dV_{IN}}{dt}$$

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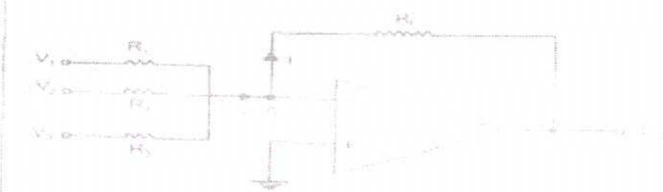
<tr><td>IX(b)</td><td>



Explanation & Derivation

$$i = i_1 + i_2 + i_3 + \cdots\cdots i_n$$

$$\Rightarrow i = \frac{v_1 - 0}{R_1} + \frac{v_2 - 0}{R_2} + \frac{v_3 - 0}{R_3} + \cdots\cdots + \frac{v_n - 0}{R_n}$$

$$\Rightarrow i = \frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} + \cdots\cdots\cdots + \frac{v_n}{R_n} \cdots\cdots\cdots (i)$$

$$i = \frac{0 - v_0}{R_f} = -\frac{v_0}{R_f} \cdots\cdots\cdots (ii)$$

$$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} + \cdots\cdots + \frac{v_n}{R_n} = -\frac{v_0}{R_f}$$

$$\Rightarrow v_0 = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \frac{R_f}{R_3}v_3 + \cdots\cdots\cdots + \frac{R_f}{R_n}v_n\right)$$

</td><td>3

4</td><td>7</td></tr>
<tr><td>X(a)</td><td></td><td>4</td><td>8</td></tr>
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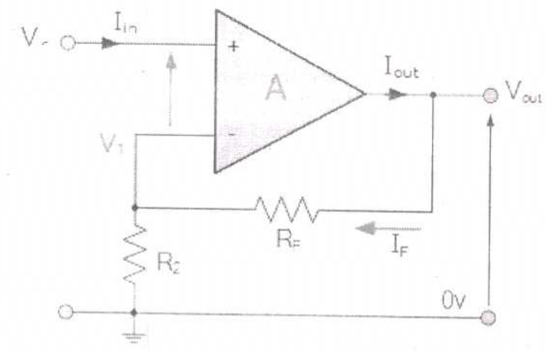


Non-inverting Operational Amplifier Gain

Non-inverting Operational Amplifier Gain

$$V_1 = \frac{R_2}{R_2 + R_F} V_{OUT}$$

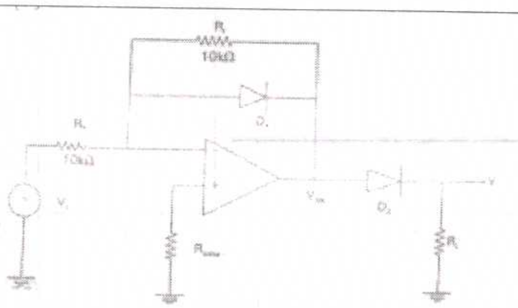
Ideal Summing Point: $V_1 = V_{IN}$

Voltage Gain, $A_{(V)}$ is equal to: $\frac{V_{OUT}}{V_{IN}}$

Then, $A_{(V)} = \frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_F}{R_2}$

Transpose to give: $A_{(V)} = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_F}{R_2}$

Then the closed loop voltage gain of a **Non-inverting Operational Amplifier** will be given as:

$$A_{(V)} = 1 + \frac{R_F}{R_2}$$
</td><td>4</td><td></td></tr>
<tr><td>X(b)</td><td>


The combination of op amp and diode(precision diode) acts as diode with zero cut in voltage.For normal silicon diodes there exists a dead time when the voltages are within (0< Vd< Vcutin voltage). Because of high gain
</td><td>4

3</td><td>7</td></tr>
</table>

	of op amps even for very small input voltages in rising mode the output will be high and the dead time can be made negligible. A précision diode has a practical zero cut in voltage. When Vi is positive diode D1 conduct D2 reverse biased hence Vo is zero when Vi is negative D2 conduct but D1 is off. circuit acts like inverter if RF=R1 with Vo positive		