SET-2

33

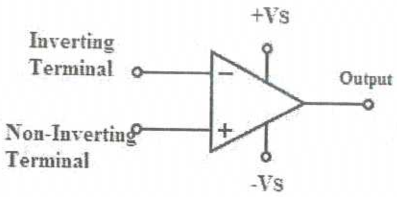
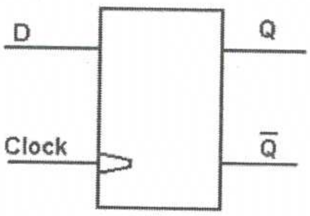
8/11/23

SCORING INDICATORS

11 Nov-23

COURSE NAME: ANALOG & DIGITAL CIRCUITS
COURSE CODE: TED (21) - 3031

QID:

<table>
<tr><th>Q No.</th><th>Scoring Indicator</th><th>Split Score</th><th>Sub Total</th><th>Total Score</th></tr>
<tr><td></td><td>PART A</td><td></td><td></td><td>9</td></tr>
<tr><td>I.1</td><td>RC coupling</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>I.2</td><td>Over all Gain = $\frac{A}{1-\beta}$</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>I.3</td><td>
</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>I.4</td><td>Op-amp precision rectifier has no voltage drop due to diode potential barrier, so can be used to rectify signals below 0.7 volts.</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>I.5</td><td>2 is 0010
5 is 0101
So BCD of 25 is 00100101</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>I.6</td><td>Exclusive NOR (XNOR)
<table>
<tr><th>A</th><th>B</th><th>A XNOR B</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table></td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>I.7</td><td>$Y = \overline{A(B+C)} = \overline{A} + \overline{(B+C)} = \overline{A} + \overline{B}\,\overline{C}$</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1.8</td><td>
</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1.9</td><td>The modulus of a decade counter is 10</td><td>1</td><td>1</td><td>1</td></tr>
</table>

<table>
<tr><th>Q No.</th><th>Scoring Indicator</th><th>Split Score</th><th>Sub Total</th><th>Total Score</th></tr>
<tr><td></td><td>PART B</td><td></td><td></td><td>24</td></tr>
<tr><td>II.1</td><td>

Class	A	B	C
Conduction Angle	360°	180°	Less than 90°

</td><td>1 for each</td><td>3</td><td>3</td></tr>
<tr><td>II.2</td><td>Barkhausen's Criteria for sustained oscillations:
1. The product of the gain in the amplifier and the feedback factor must equal unity.
$$|A\beta| = 1$$
2. Total phase shift around the loop should be zero.</td><td>1

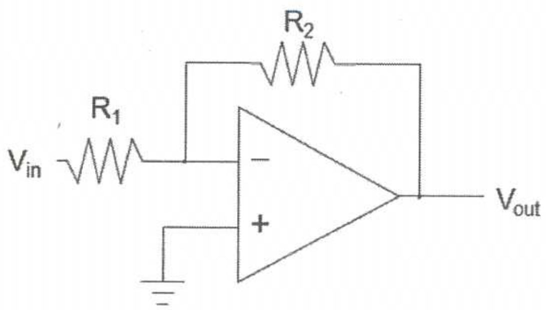
1
1</td><td>3</td><td>3</td></tr>
<tr><td>II.3</td><td>Three essential elements of oscillators
• A tank circuit or noise signal
• An amplifier.
• A positive feedback.</td><td>1 each</td><td>3</td><td>3</td></tr>
<tr><td>II.4</td><td>

Astable	Bistable
No stable state	Two stable state
No trigger needed	Trigger needed
Used as pulse generators	Used as flip flops

</td><td></td><td></td><td></td></tr>
<tr><td>II.5</td><td>

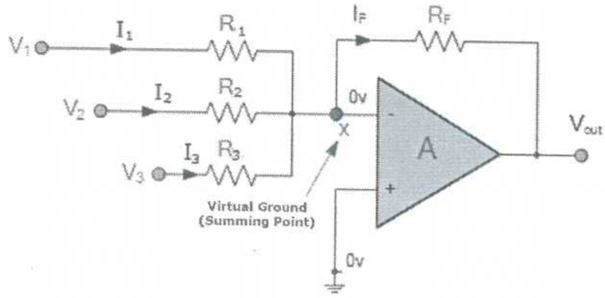
Property	Practical(Typical)
Open-loop gain	Very high (>10000)
CMRR	High (> 60 dB)
Input Resistance	High (>1 MΩ)
Output Resistance	Low(< 100 Ω)
Input Bias Currents	Low (< 50 nA)
Offset Voltages	Low (< 10 mV)
Offset Currents	Low (< 50 nA)
Slew Rate	A few V/μs
Drift	Low

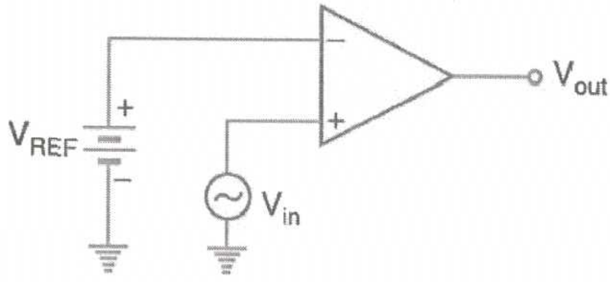
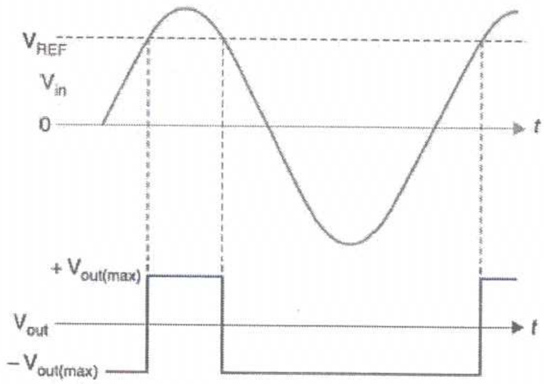
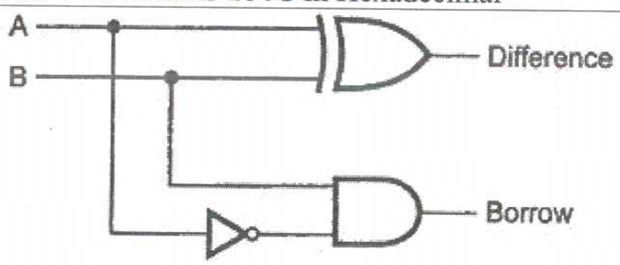
(Any 3 points only)</td><td>1 each</td><td>3</td><td>3</td></tr>
<tr><td>II.6</td><td>

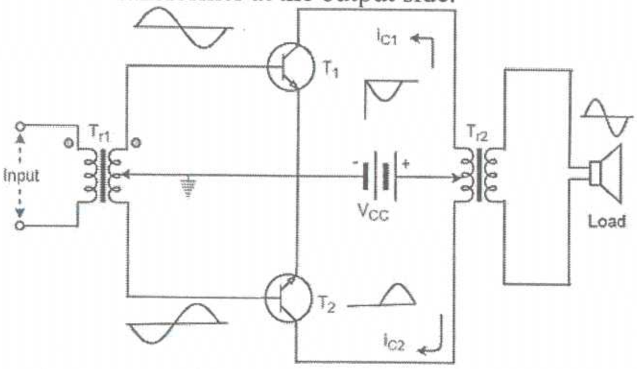
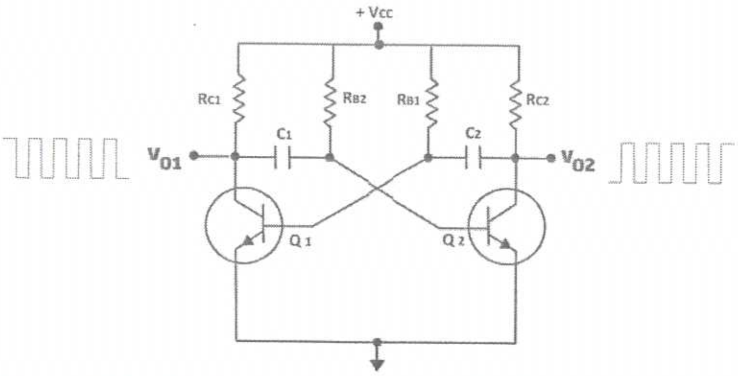


$$\boxed{v_o = -\frac{R_2}{R_1} v_{in}}$$

</td><td>2 Marks for Circuit & 1 Marks for equation</td><td>3</td><td>3</td></tr>
</table>

II.7	Inverting Summing Amplifier  $I_F = I_1 + I_2 + I_3$ -Equation-1 We have, $I_1 = \frac{V_1 - 0}{R_1} = \frac{V_1}{R_1}$ $I_2 = \frac{V_2 - 0}{R_2} = \frac{V_2}{R_2}$ $I_3 = \frac{V_3 - 0}{R_3} = \frac{V_3}{R_3}$ $I_F = \frac{0 - V_o}{R_F} = -\frac{V_o}{R_F}$ Substituting these in Equation 1, we get $-\frac{V_o}{R_F} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$ $\boxed{V_o = -R_F \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]}$ If all resistors are of equal resistance then $V_o = -(V_1+V_2+V_3)$	1 2	3	3

<table>
<tr><td>II.8</td><td>Positive Voltage level detector

</td><td>1</td><td>3</td><td>3</td></tr>
<tr><td></td><td>When a comparator is used to detect level of a signal with a dc reference signal, then the circuit is called a positive level detector. Whenever input voltage goes above the dc reference voltage, the output will be positive saturation voltage and if voltage is below dc reference voltage output will be negative saturation.</td><td>1</td><td></td><td></td></tr>
<tr><td></td><td>
</td><td>1</td><td></td><td></td></tr>
<tr><td>II.9</td><td><table>
<tr><td>16</td><td>5708</td><td></td></tr>
<tr><td>16</td><td>356</td><td>R=12 =C</td></tr>
<tr><td>16</td><td>22</td><td>R=4</td></tr>
<tr><td>16</td><td>1</td><td>R=6</td></tr>
<tr><td></td><td>0</td><td>R=1</td></tr>
</table>
5708 in decimal is 164C in Hexadecimal</td><td>3</td><td>3</td><td>3</td></tr>
<tr><td>II.10</td><td>
</td><td>1</td><td>3</td><td>3</td></tr>
<tr><td></td><td><table>
<tr><th colspan="2">Inputs</th><th colspan="2">Outputs</th></tr>
<tr><td>A</td><td>B</td><td>Difference</td><td>Borrow</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td></tr>
</table></td><td>2</td><td></td><td></td></tr>
</table>

Q No.	Scoring Indicator	Split Score	Sub Total	Total Score
	PART C			42
III.1	Push-Pull amplifier is a combination of two class B power amplifiers. It has two identical npn transistors with their emitters connected together. Also, it employs a central tapped transformer at input to provide opposite polarity input to the two transistors and a transformer at the output side.	2	7	7
		3		
	When a signal is given to the input transformer, during positive half cycle the transistor T1 gets positive base voltage and it conducts current in the opposite direction to the input side of output transformer. The induced output voltage of transformer will be in phase with actual input signal. Similarly, transistor T2 will conduct when input signal is negative. Thus, T1 pushes signal high during positive half cycle and T2 pulls signal low during negative half cycle.	2		
	OR			
III.2		3	7	7
	• Let us assume that Q_2 turns ON first and Q_1 is OFF. Then capacitor C_1 **gets charged from V_{CC} via R_{C1} and Q_2**. Also, capacitor C_2 **gets charged from V_{CC} via R_{B1} and Q_2**. Since collector resistances has smaller values compared to base resistance, **C_1 gets charged faster than C_2**. In this process the **left plates** of capacitors are **positive** and right plates are **negative**. • The output across Q_1, $V_{O1}=V_{CC}$ and output across Q_2, $V_{O2}=0$. • When Q_2 is ON the capacitor C_2 gets connected between base and emitter of Q_1. When voltage across C_2 reaches a minimum value of 0.7V, Q_1 turns ON. And as soon as Q_1 turns ON, the voltage across C_1 becomes base emitter voltage for Q_2, which is a negative voltage, so Q_2 turns OFF. • Now Q1 is ON and Q_2 is OFF. Then capacitor C_1 gets charged from V_{CC} via R_{B2} and Q_1. Also, capacitor C_2 gets charged from V_{CC} via R_{C2} and Q_1. Since collector resistances has smaller values compared to base resistance, C_2 gets charged faster than C_1. In this process the right plates of capacitors are positive and left plates are negative. • The output across Q_2, $V_{O2}=V_{CC}$ and output across Q_1, $V_{O1}=0$. • When the capacitor C_1 gets a minimum voltage of 0.7V, then it turns ON transistor Q_2. And as soon as Q_2 turns ON, the voltage across C_2 becomes base emitter voltage for Q_1, which is a negative voltage, so Q_1 turns OFF.	4		

<table>
<tr><th>Q No.</th><th>Scoring Indicator</th><th>Split Score</th><th>Sub Total</th><th>Total Score</th></tr>
<tr><td>III.3</td><td>

i. **Band Width**

The operational amplifiers bandwidth is the frequency range over which the voltage gain of the amplifier is above 70.7%. An ideal op-amp has infinite band width.

ii. **CMMR**

The CMRR stands for Common Mode Rejection Ratio. It is the ratio of differential mode gain to common mode gain of op-amp. CMMR determines how good is an opamp in rejecting input signal that are common to both terminals. For an ideal op-amp CMMR is infinite.

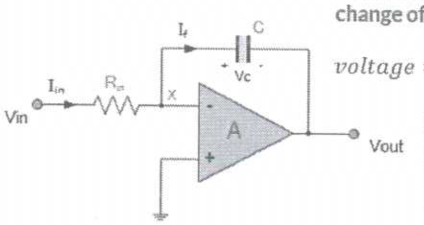
iii. **Slew Rate**

Slew rate is defined as the maximum rate of change of an op-amps output voltage, and is given in units of volts per microsecond. Ideally op-amp as infinite voltage changes per microsecond.

</td><td>2

3

2</td><td>7</td><td>7</td></tr>
<tr><td></td><td>**OR**</td><td></td><td></td><td></td></tr>
<tr><td>III.4</td><td>



When the capacitor is charging and discharging, the rate of change of voltage across the capacitor is given as:

$$voltage = \frac{1}{C}\int (current)dt \quad V_c = \frac{1}{C}\int I_f dt = \frac{1}{C}\int I_{in} dt$$

$$I_{in} = \frac{V_{in} - V_x}{R_{in}} = \frac{V_{in} - 0}{R_{in}} = \frac{V_{in}}{R_{in}}$$

$$V_c = \frac{1}{C}\int \frac{V_{in}}{R_{in}} dt = \frac{1}{CR_{in}}\int V_{in} dt$$

Voltage across capacitor can also be found as:

$$V_C = V_x - V_o = 0 - V_o = -V_o$$

So,

$$-V_o = \frac{1}{CR_{in}}\int V_{in} dt$$

1. Negative feedback forces the op-amp to produce an output voltage that maintains a virtual earth at the op-amp's inverting input. (Vx=0v)
2. Due to large input resistance input current is equal to feedback current (Iin=If)

If we take Rin as R, then final equation for output voltage is:

$$\boxed{V_o = -\frac{1}{RC}\int V_{in} dt}$$

The constant RC is called time constant

</td><td>3 Marks for Circuit and 3 Marks for derivation
1 Mark for final Equation</td><td>7</td><td>7</td></tr>
</table>

<table>
<tr><th>Q No.</th><th>Scoring Indicator</th><th>Split Score</th><th>Sub Total</th><th>Total Score</th></tr>
<tr><td>III.5</td><td>

Steps to do subtractions using 2’s complement method (Ex: For A-B)

1. Convert A and B to its binary form.
2. Make both A and B binary form in to equal bit size by appending required zeros at left end.
3. Add a ‘0’ as sign bit at left side of both A and B.
4. Convert the negative numbers (in this question -B only) to its 2’s complement form. For this first we have to find its 1’s complement and then add ‘1’ to it.
5. Add A to 2’s complement of (-B).
6. Ignore any carry generated.
7. Check sign bit of the result.
    a. If Sign bit is ‘0’ then the result is positive and is in true form.
    b. If Sign bit is ‘1’ then the result is negative and is in its 2’s complemented form. True form should be found.

Covert 35 in to binary

<table>
<tr><td>2</td><td>35</td><td></td></tr>
<tr><td>2</td><td>17</td><td>R=1</td></tr>
<tr><td>2</td><td>8</td><td>R=1</td></tr>
<tr><td>2</td><td>4</td><td>R=0</td></tr>
<tr><td>2</td><td>2</td><td>R=0</td></tr>
<tr><td>2</td><td>1</td><td>R=0</td></tr>
<tr><td></td><td>0</td><td>R=1</td></tr>
</table>

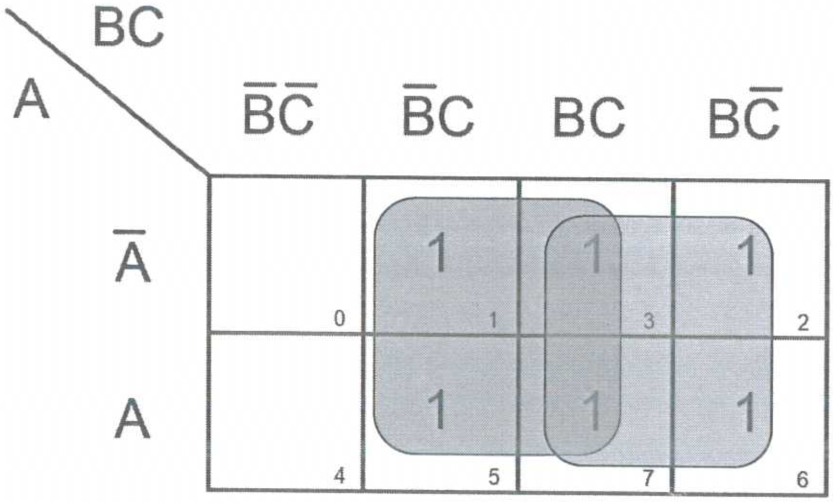
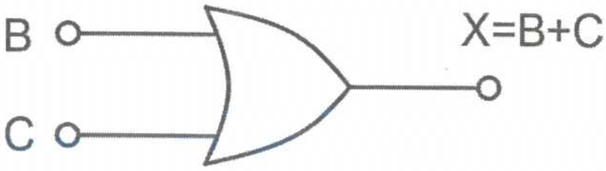
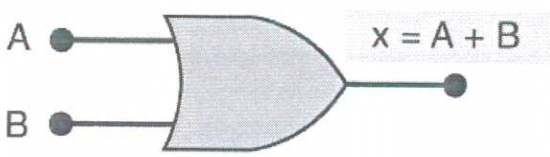
Binary Value of 35 = 100011
Binary Value of 12 = 1100
Since 35 need 6 bits in binary, 12 also need to be in 6 bits form.
Hence Binary Equivalent of 12 = 001100
Now Add sign bit to both 35 and 12
35 = 0100011 and 12=0001100
Negative number should be in 2’s complement form
1’s complement of 12 is = 1110011
2’s complement of 12 = 1110011
+ 1
1110100

Now 35-12 is same as 35+(2’s complement of 12)
0001100
+ **1110100**
1 0010111
The carry 1 is ignored. In the result 0010111 The sign bit is 0. So, the result **0010111** is positive and in actual form.
Decimal equivalent of 0010111 is
$1\times2^4+1\times2^2+1\times2^1+1\times2^0=$ **23**

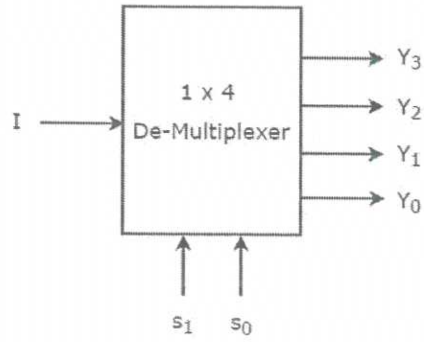
</td><td>1
1
1
1
1
1
1</td><td>7</td><td>7</td></tr>
<tr><td></td><td>OR</td><td></td><td></td><td></td></tr>
<tr><td>III. 6</td><td>

<table>
<tr><th>A \ BC</th><th>$\bar{B}\bar{C}$</th><th>$\bar{B}C$</th><th>BC</th><th>$B\bar{C}$</th></tr>
<tr><td>$\bar{A}$</td><td>0</td><td>1 (1)</td><td>1 (3)</td><td>1 (2)</td></tr>
<tr><td>A</td><td>4</td><td>1 (5)</td><td>1 (7)</td><td>1 (6)</td></tr>
</table>

</td><td>2</td><td>7</td><td>7</td></tr>
</table>

	 $\mathbf{X = B + C}$  	2 1 2		
III.7	i. Basic Gates 1. OR Gate Y=A+B 2. AND Gate Y=A+B 3. NOT Gate Y=A' ii. Universal Gates 1. NOR Gate Y=(A+B)' 2. NAND Gate Y=(AB)' iii. Exclusive Gates 1. XOR gate Y=AB'+A'B 2. XNOR gate Y=AB+A'B'	1 for each	7	7
	OR			
III.8	$X = A + \bar{A}B + BA = (A + \bar{A})(A + B) + BA$ $= A + B + BA$ $= A + (1 + A)B$ $X = A + B$  	4 3	7	7

III.9 | 1 | 7 | 7



2

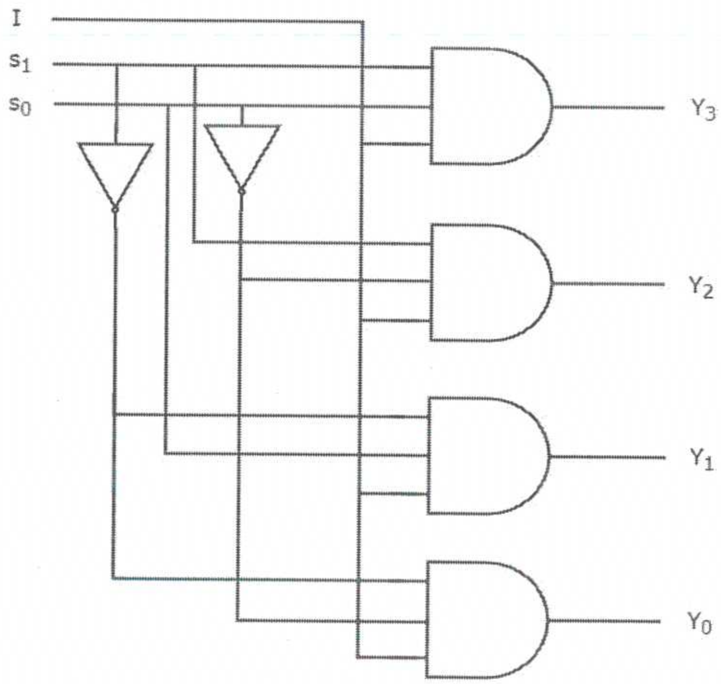
De-Multiplexer is a combinational circuit that performs the reverse operation of Multiplexer. It has single input, ‘n’ selection lines and maximum of 2^n outputs. The input will be connected to one of these outputs based on the values of selection lines.

Since there are ‘n’ selection lines, there will be 2^n possible combinations of zeros and ones. So, each combination can select only one output. De-Multiplexer is also called as **De-Mux**. 1x4 De-Multiplexer has one input I, two selection lines, s_1 & s_0 and four outputs Y_3, Y_2, Y_1 &Y_0.

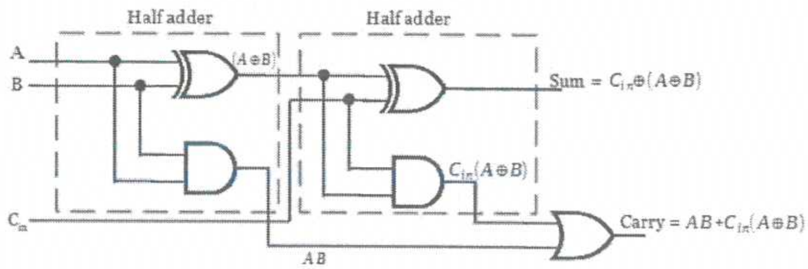
2

Selection Inputs		Outputs			
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

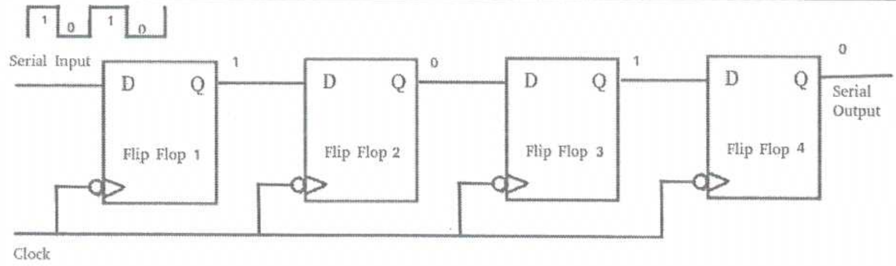
2



OR

III.10	The full adder can be implemented with two half adders by cascading them. The sum output of first half adder is Ex-OR of A and B. The sum output of full adder is Ex-OR of Cin and output of first half adder. The carry output of the full adder can be realized as below from the obtained boolean expression. Refer Postulates and Theorems of Boolean Algebra for the below simplification. $\text{Carry} = AB+AC_{in}+BC_{in}$ $= AB+AC_{in}(B+\bar{B})+BC_{in}(A+\bar{A})$ $= AB+ABC_{in}+A\bar{B}C_{in}+ABC_{in}+\bar{A}BC_{in}$ $= AB(1+C_{in}+C_{in})+A\bar{B}C_{in}+\bar{A}BC_{in}$ $= AB+A\bar{B}C_{in}+\bar{A}BC_{in}$ $= AB+C_{in}(A\bar{B}+\bar{A}B)$ $= AB+C_{in}(A\oplus B)$ $A+A=A$ $1+A=1$ The full adder can be realized as below. The truth table for the below full adder circuit is the same as the one discussed above.  *Realization of full adder with two half adders*	3 4	7	7

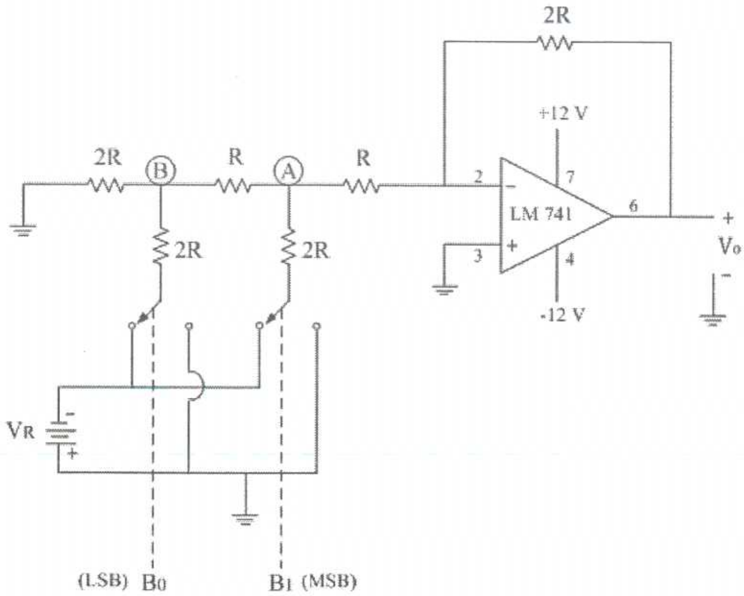
<table>
<tr><th>Q No.</th><th>Scoring Indicator</th><th>Split Score</th><th>Sub Total</th><th>Total Score</th></tr>
<tr><td>III.11</td><td>



Serial-In Serial-Out Shift Register (SISO)

The shift register, which allows serial input (one bit after the other through a single data line) and produces a serial output is known as Serial-In Serial-Out shift register. Since there is only one output, the data leaves the shift register one bit at a time in a serial pattern. The circuit consists of four D flip-flops which are connected in a serial manner. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop. The circuit takes the serial data input from the left side of the flip flop and transmit to right one bit at a time when a falling edge of clock pulse is detected. The main use of a SISO is to act as a delay element.

</td><td>4
3</td><td>7</td><td>7</td></tr>
<tr><td></td><td>OR</td><td></td><td></td><td></td></tr>
<tr><td>III.12</td><td>



R-2R ladder type DAC

The circuit diagram shows the basic 2 bit R-2R ladder DAC circuit using op-amp. Here only two values of resistors are required i.e. R and 2R. The number of digits per binary word is assumed to be two (i.e. n = 2). The switch positions decides the binary word (i.e. B1 B0). The typical value of feedback resistor is Rf = 2R. The resistance R is normally selected any value between 2.5 kΩ to 10 kΩ. Using the properties of op-amp, the generalized analog output voltage equation can be given as:

$$V_o = -V_R \frac{R_f}{R}\left[\frac{B_1}{2^1}+\frac{B_2}{2^2}+\frac{B_3}{2^3}+----+\frac{B_n}{2^n}\right]$$

Thus, a voltage corresponding to the binary value fed as input will be generated as output.

</td><td>3
3
1</td><td>7</td><td>7</td></tr>
</table>