SCHEME OF VALUATION

(Scoring Indicators)

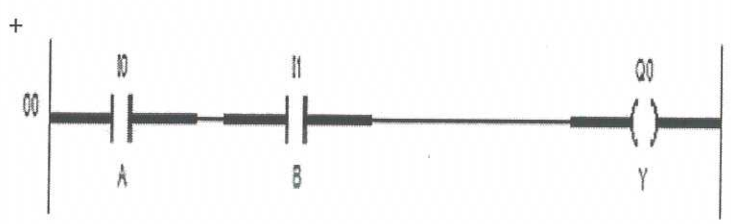
REVISION : 15 | COURSE CODE :TED(15)-6032

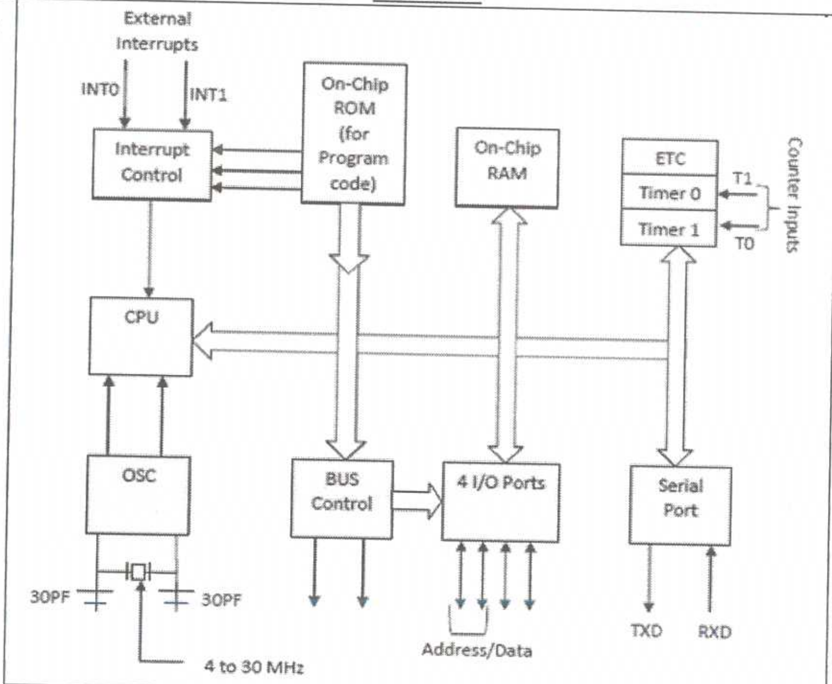
COURSE TITLE: MICROCONTROLLER AND PROGRAMMABLE LOGIC CONTROLLERS

VERSION :A

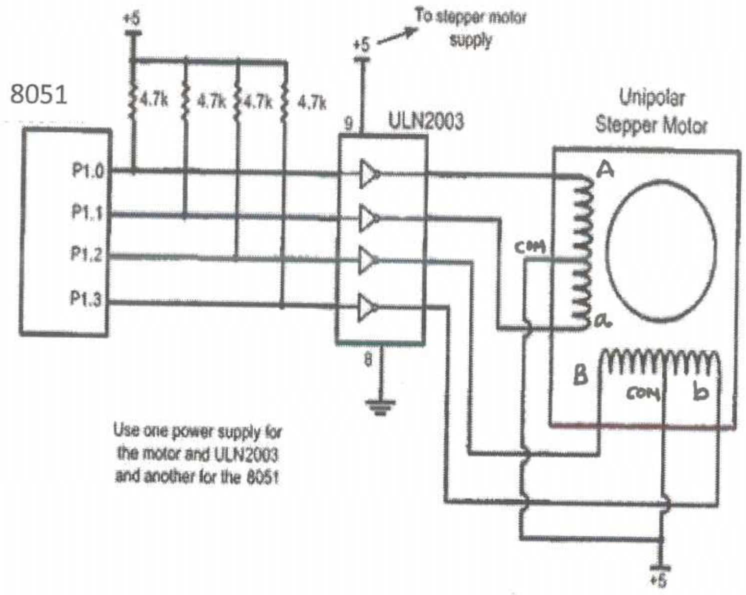
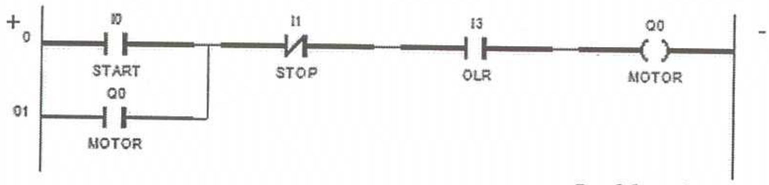
QN NO		SCORING INDICATORS	SPLIT UP SCORE	SUB TOTAL	TOTAL SCORE
I		**PART A**			
	1.	Microcontroller is a programmable semiconductor device available as IC and capable of performing arithmetic and logical operations. It contains CPU, a fixed amount of RAM, ROM, I/O ports and Timer all on a single chip.	1 x 2	2	
	2.	CY- Carry Flag AC-Auxiliary Carry Flag OV- Overflow Flag P- Parity Flag	4 x 0.5	2	
	3	(i)MOV A, #15 H-----------Immediate Addressing (ii)MOVX A, @DPTR-----Register Indirect Addressing	2 x 1	2	

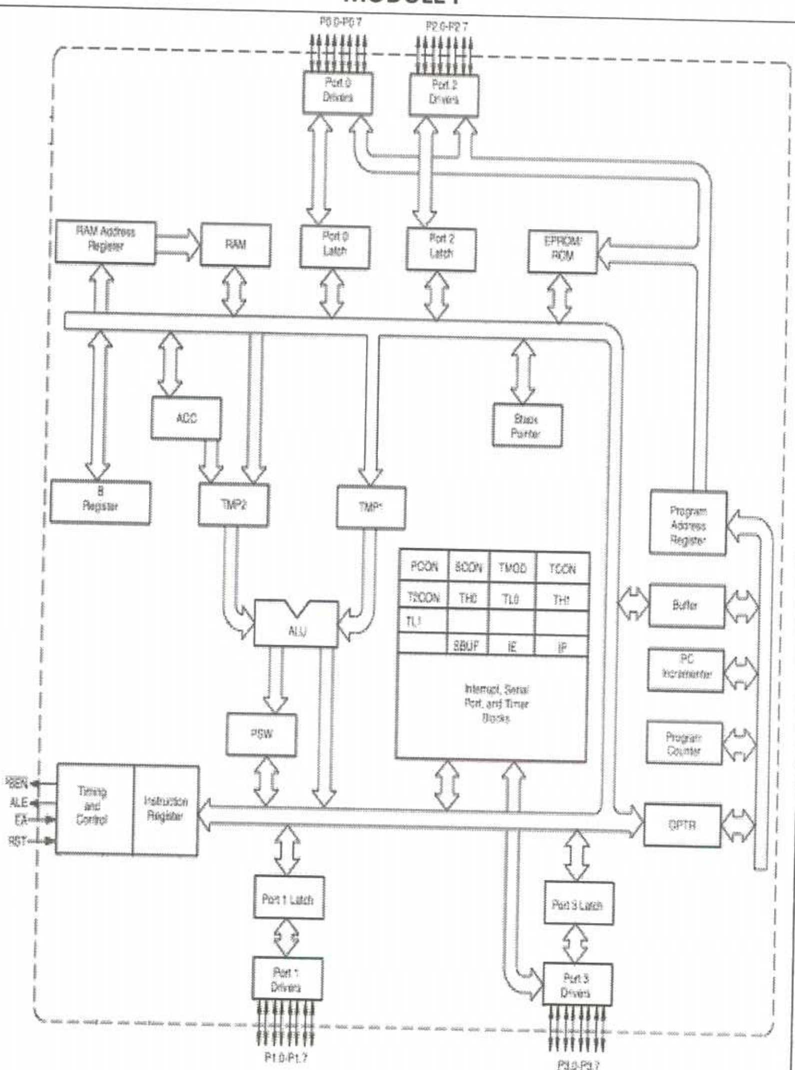
	4	• High Performance 8-Bit MCU
		• RISC Architecture
		    • 32 Registers
		    • 2-Address Instructions
		    • Single Cycle Execution
		• Large linear address spaces
		• Efficient C Language Code Density
		• On-chip in-system programmable memories
		(Any Two)
			2 x 1	2	

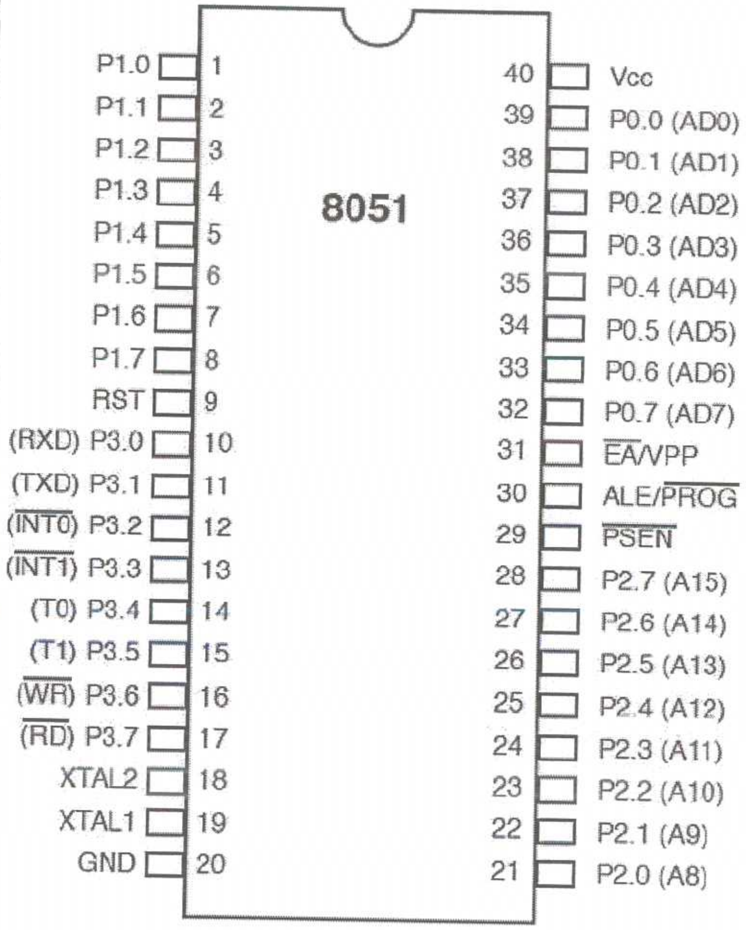
	5.	 *Ladder diagram* *Labelling*	1 1	2	10

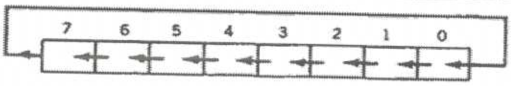
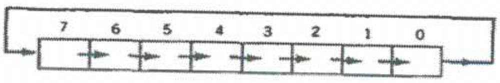
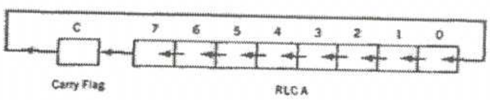
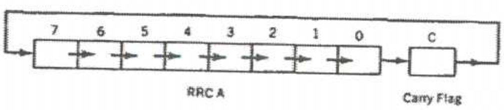
QN NO		SCORING INDICATORS	SPLIT UP SCORE	SUB TOTAL	TOTAL SCORE
II		PART B			
II	1.		4		
		CPU • Responsible for all arithmetic, computation and logical operations Internal Memory • Internal RAM :Capacity : 128 Bytes • Internal ROM:Capacity : 4 K Bytes I/O PORTS • 4 Nos : P0, P1, P2, P3 • Capacity : 8 bit each (8bit X 4 = 32 bits) SERIAL PORTS • full duplex serial port. TIMERS/COUNTERS • generate accurate time delay • used as external counters • 2 Nos: T0, T1 • Capacity : 16 bit each (16 bit X 2 Nos = 32 bits) OSCILLATOR SECTION • Generate clock pulses for synchronizing the internal operations in the micro controller. • Internal frequency 1-16 MHz INTERRUPT CONTROL • Responds to specific external / internal events BUS CONTROL o Address Bus- unidirectional o Data Bus – bidirectional o Control Bus - bidirectional	2	6	

QN NO		SCORING INDICATORS	SPLIT UP SCORE	SUB TOTAL	TOTAL SCORE
		PART B			
II	2	Features of 8051 Microcontroller • ALU - 8 Bit • RAM - 128 Bytes • ROM - 4 KB • I/O lines - 4 No X 8 bit = 32 bits • Timer - 2 No X 16 bit =32 bit • Program memory - 64 KB • Data memory - 64 KB • Clock -12 MHz • Serial port -1 No (FULL DUPLEX) • Interrupt source - 5 Nos On chip oscillator and clock circuitry (Any six)	1 X 6	6	
II	3	ANL ANL Destination, Source [Destination] ← [Destination] ANDed with [Source] SOURCE --8 bit data,8 BIT ADDRESS,R0-R7,@R0,@R1 DESTINATION-A, 8 BIT ADDRESS	1		
		EG : ANL A, R0 [A] ← [A] ANDed [R0]	1		
		ORL ORL Destination, Source [Destination] ← [Destination] ORed with [Source] SOURCE --8 bit data,8 BIT ADDRESS,R0-R7,@R0,@R1 DESTINATION-A, 8 BIT ADDRESS	1		
		EG : ORL A, R0 [A] ← [A] ORed [R0]	1		
		XRL XRL Destination, Source [Destination] ← [Destination] XORed with [Source] SOURCE --8 bit data,8 BIT ADDRESS,R0-R7,@R0,@R1 DESTINATION-A, 8 BIT ADDRESS	1		
		EG : XRL A, R0 [A] ← [A] EXORed [R0]	1	6	

QN NO		SCORING INDICATORS	SPLIT UP SCORE	SUB TOTAL	TOTAL SCORE
II	4	 **Figure 5.11. 8051 Connection to Stepper Motor** *Diagram* *Labelling* (Variations may accept)	 4 2	6	
II	5	**<u>Features of the PIC18 microcontroller</u>** • High Performance RISC CPU • 8-bit CPU • 2 MB program memory space • 256 bytes to 1KB of data EEPROM • 10-bit A/D converter *(Any Four)*	1.5 x 4	6	
II	6	 *Ladder diagram* *labelling* *Ladder diagram using other PLC language also can accept*	 4 2	6	
II	7	• Types of I/O required • The number of I/O points required per module • Isolation required between the controller and the target process • Future needs of the plant in terms of *spare* I/O points; • Power supply requirements of I/O points • Size of memory required; • Speed and power required of the CPU and instruction set • Manufacturer's support and backup. *(Any 6)*	1 x 6	6	30

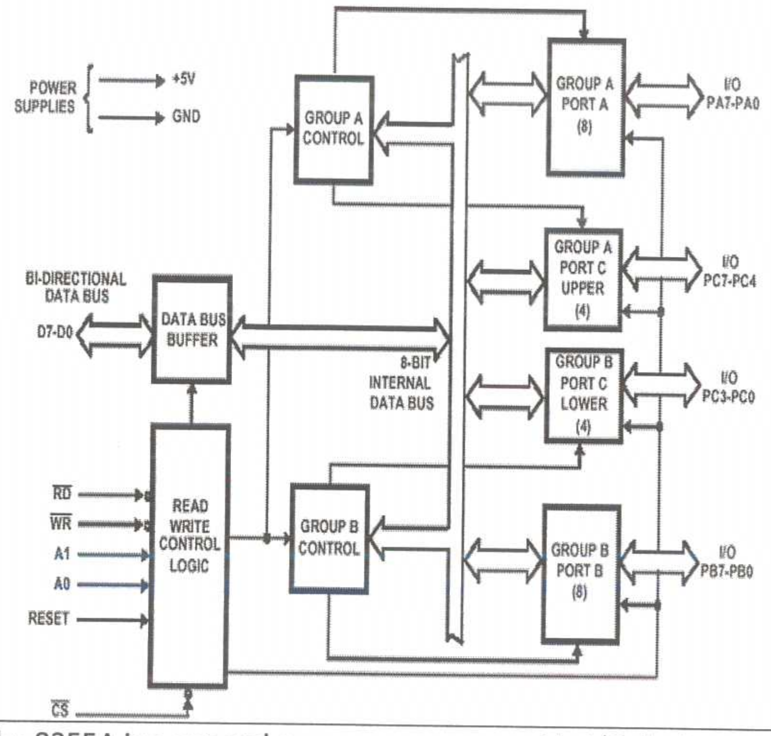
QN NO		SCORING INDICATORS	SPLIT UP SCORE	SUB TOTAL	TOTAL SCORE
		PART C			
		MODULE I			
III	a	 *Fig* *Labelling*	6 3	9	
III	b	**ALU** • Arithmetic and Logic Unit • Responsible for all arithmetic, computation and logical operations **DPTR** • Data Pointer Register • 16 bit register • Responsible for all 16 bit data transfer operations and involves in external data transfer **Program Counter** • 16 bit register • It points to the address of the next instruction to be executed **B register** • 8bit register • Assists A register in multiplication and division operations	1.5 x 4	6	15

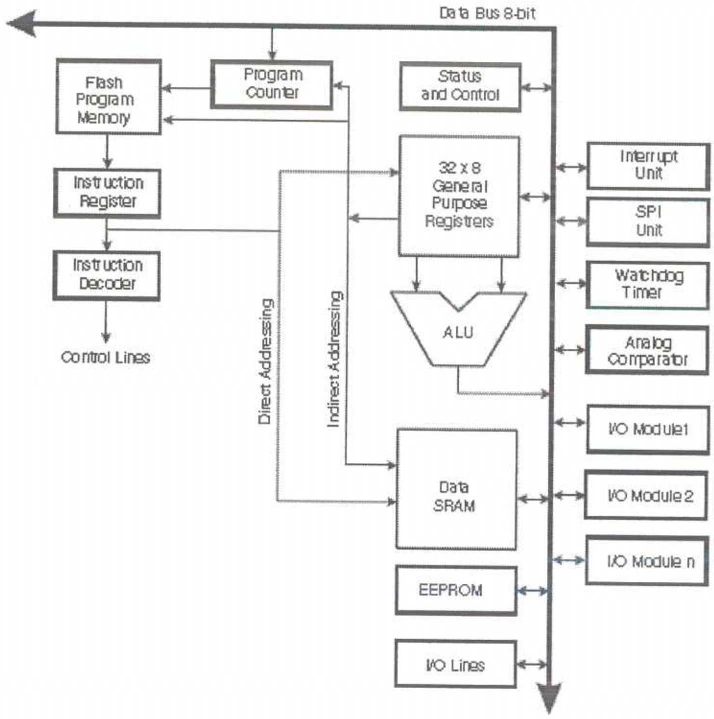
QN NO		SCORING INDICATORS	SPLIT UP SCORE	SUB TOTAL	TOTAL SCORE
IV	a		9		
		For partialy completed diagram following scheme can be used			
		40 Pins marked without alternate naming given in bracket	(6)		
		4 Ports only	4 x 0.75= (3)		
		4 Ports with alternate functions	4 x 1.5= (6)		
		VCC, GND, XTAL 1, XTAL2	(2)		
		PSEN,ALE,EA	(1)	9	
IV	b	• An interrupt is an external or internal event that interrupts the normal operation of a microcontroller	1		
		5 Interrupts in 8051 (with order of normal priority) 1. External hardware interrupts $\overline{INT0}$ 2. Timer 0 overflow interrupt T0 3. External hardware interrupts $\overline{INT1}$ 4. Timer 1 overflow interrupt T1 5. Serial interrupt (TI & RI)	5	6	15

QN NO		SCORING INDICATORS	SPLIT UP SCORE	SUB TOTAL	TOTAL SCORE
		MODULE II			
V	a	(i) MOV R0, #0A5H [R0]=A5 H	1		
		(ii) ADD A, # 1C H [A] ←----- [A] + 1C H	1		
		(iii) PUSH 00H [SP]←-----[SP]+1 [INT MEMORY @ SP] ←----[R0]	1		
		(iv) XCH A, R7 [A] ←---→ [R7]	1		
		(v) INC DPTR [DPTR] ←--- [DPTR] +1	1		
		(vi) CLR A [A]= 00 H	1		
		(vii) ORL A, R1 [A] ←----- [A] LOGICAL OR [R1]	1		
		(viii) DEC 15H [15] ←----- [15] - 01 H	1	8	
V	b	PURPOSE :Used to Perform data rotation	1		
		 RL A  RRA  RLC A  RRC A *Example for each*	1 x 4 0.5 x 4	7	15

QN NO		SCORING INDICATORS	SPLIT UP SCORE	SUB TOTAL	TOTAL SCORE
VI	a	To store and retrieve data during program execution in stack push and pop instructions are used SP: stack pointer is 8 bit register which store value of top of the stack. By default stack pointer contains 07h.	2		
		PUSH: It is used to store data into stack. During push operation stack pointer is increased first and then content of register or memory will store on that stack location which stored in SP	2		
		Eg: PUSH 00 H [INT MEMORY @ SP] ←----[R0]	1		
		POP: It is used to retrieve data from stack. In this case retrieve data first and then stack pointer is decreased by one.	2		
		Eg: POP 00 H [R0] ←------ [INT MEMORY @ SP] [SP]←-----[SP]-1	1	8	

QN NO		LABEL	MNEMONICS		COMMENT	SPLIT UP SCORE	SUB TOTAL	TOTAL SCORE
VI	b		ORG	8400 H	; Start at location 8400 H			
			MOV	DPTR , #4000 H	; Load the adress of No in DPTR			
			MOVX	A ,@DPTR	; Get No in Accumulator			
			MOV	0F0 ,A	; Save No in Reg B			
			MUL	AB	; No X No			
			INC	DPTR	; Increment DPTR to point result location[LSB]			
			MOVX	@ DPTR ,A	; Save the LSB of result in result location[LSB]			
			MOV	A , 0F0	; Save MSB of result in ACC			
			INC	DPTR	; Increment DPTR to point result location[MSB]			
			MOVX	@ DPTR ,A	; Save the MSB of result in result location[MSB]			
		HALT :	SJMP	HALT	; Stay in this loop			
			END		; End of program			
					Complete program	7		
					Program without comment	(5)		
					No program but correct Flow chart /Algorithm only	(3)	7	15

QN NO		SCORING INDICATORS	SPLIT UP SCORE	SUB TOTAL	TOTAL SCORE
		MODULE III			
VII	a		6		
		The 8255A is a general purpose programmable I/O device It consists of **Ports of 8255A** 8255A has three ports, 8-bit bidirectional I/O ports (3 x 8 = 24 I/O lines) PORT A, PORT B, PORT C. Port A -contains one 8-bit output latch/buffer and one 8-bit input buffer. Port B -is similar to PORT A. Port C -can be split into two parts, PORT C lower (PC0-PC3) PORT C upper (PC7-PC4). These three ports are further divided into two groups, Group A i-ncludes PORT A and upper PORT C. Group B -includes PORT B and lower PORT C. These two groups can be programmed in three different modes, Mode 0, Mode 1 Mode 2.	2	8	

QN NO		SCORING INDICATORS	SPLIT UP SCORE	SUB TOTAL	TOTAL SCORE
VII	b	Block Diagram of the AVR MCU Architecture 	7	7	15

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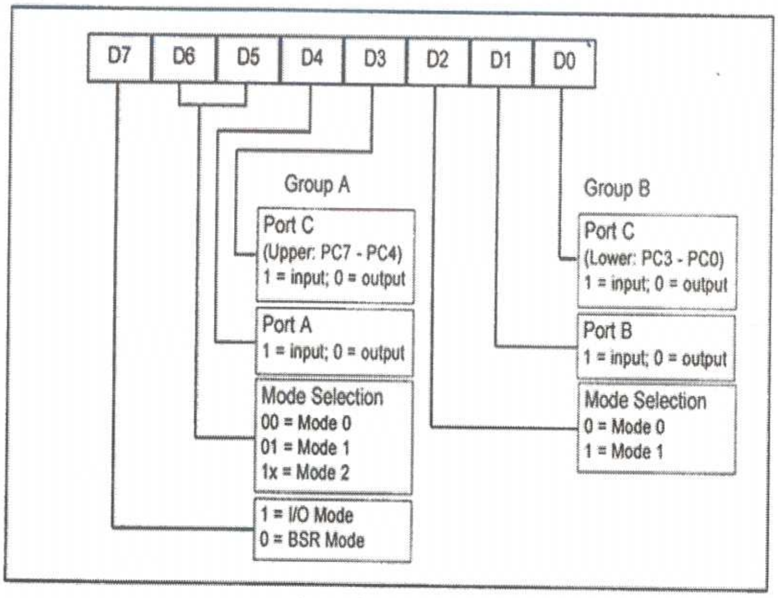
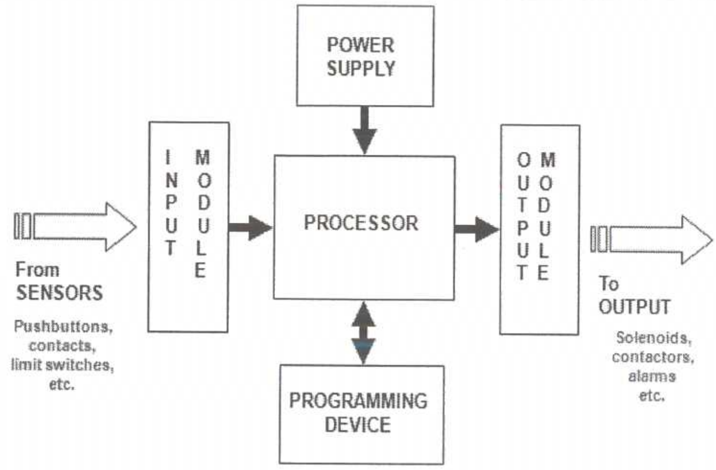
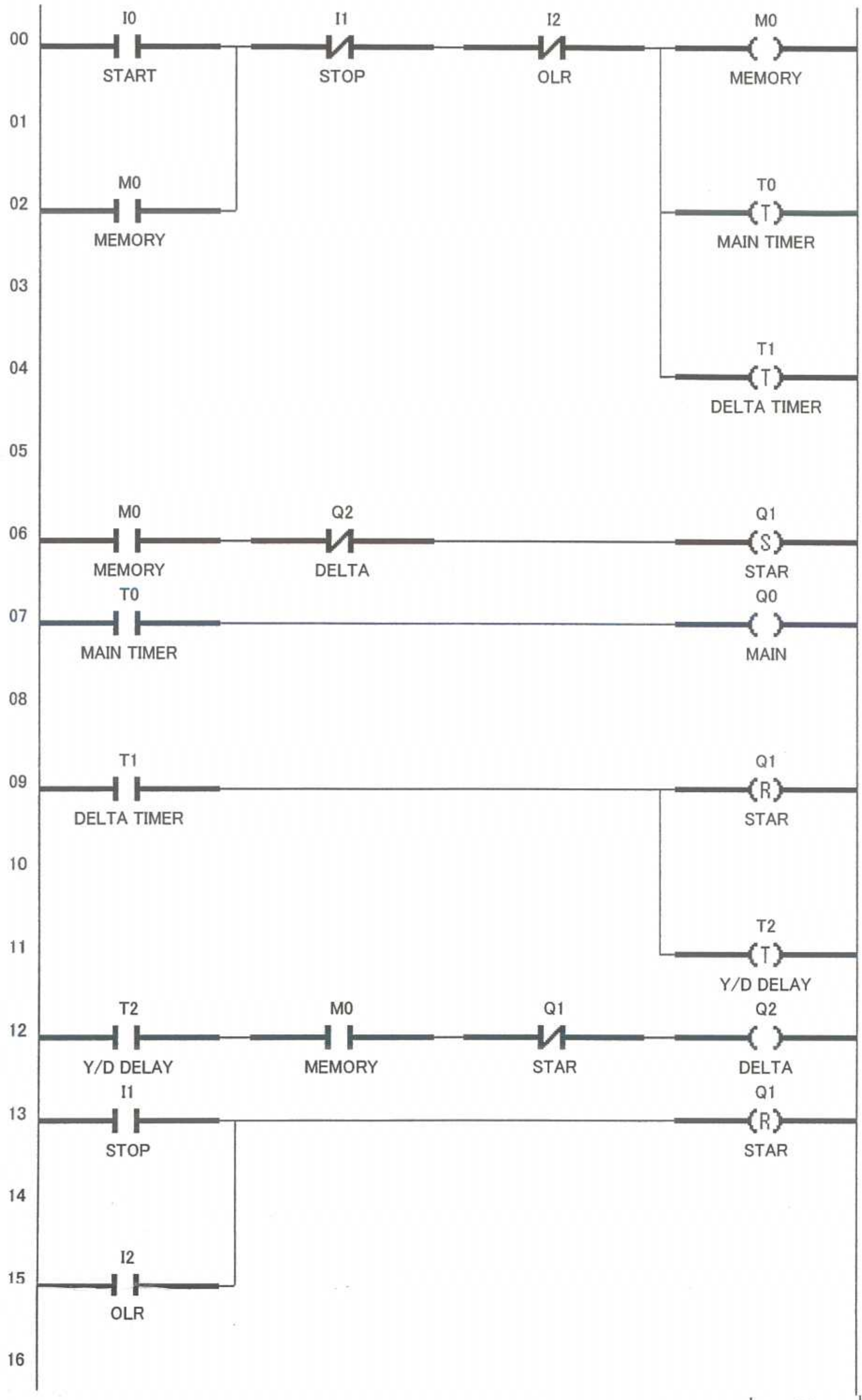
<tr><th colspan="2">QN NO</th><th>SCORING INDICATORS</th><th>SPLIT UP SCORE</th><th>SUB TOTAL</th><th>TOTAL SCORE</th></tr>
<tr><td>VIII</td><td>a</td><td><u>(i)Transmission</u> : Pin used: P3.1 (TXD)
Data written to SBUF and framed.
send via TXD line
when data has been transmitted. TI = 1 (SCON Register)</td><td>2</td><td></td><td></td></tr>
<tr><td></td><td></td><td><u>(ii)Reception</u>: Pin used: P3.0 (RXD)
Reception of serial data begins if the REN = 1 (SCON Register)(SCON.4)
Data is received by 8051 RxD line
the 8051 deframes it
places it in SBUF</td><td>2</td><td></td><td></td></tr>
<tr><td></td><td></td><td><u>(iii)Asynchronous method</u> : transfers a single byte at a time
does not need clock signal between the sender and the receiver</td><td>2</td><td></td><td></td></tr>
<tr><td></td><td></td><td><u>(iv)Data framing</u>: placing data between start bit and stop bit in serial communication</td><td>2</td><td>8</td><td></td></tr>
<tr><td>VIII</td><td>b</td><td>

Control Word Format 8255A</td><td>7</td><td>7</td><td>15</td></tr>
</table>

QN NO		SCORING INDICATORS				SPLIT UP SCORE	SUB TOTAL	TOTAL SCORE
		MODULE 1V						
IX	a	CONDITIONS	SWITCH 1	SWITCH 2	LAMP STATUS			
		1	OFF	OFF	OFF	2		
		2	OFF	ON	ON	2		
		3	ON	OFF	ON	2		
		4	ON	ON	OFF	2	8	
IX	b					5		
		PROCESSOR • Control Portion of the PLC • Provides intelligence to command and govern the activities of the entire PLC systems. **PROGRAMMING DEVICE** • Used to enter the desired program that will determine the sequence of operation **I/O Module** • Input module + Output module • The I/O interface section of a PLC connects it to external field devices.				2	7	15
X	a	Parameter	Conventional panel board	PLC System				
		Price per function	Fairly low	Low				
		Physical size	Bulky	Very compact				
		Operating speed	Slow	Fast				
		Electrical noise immunity	Excellent	Good				
		Installation	Time-consuming to design and install	Simple to program and install				
				Any 4		2 x 4	8	

<table>
<tr><th colspan="2">QN NO</th><th>SCORING INDICATORS</th><th>SPLIT UP SCORE</th><th>SUB TOTAL</th><th>TOTAL SCORE</th></tr>
<tr><td>X</td><td>b</td><td>
</td><td>7</td><td></td><td></td></tr>
<tr><td></td><td></td><td>Ladder diagram written using other PLC languages can also be accepted</td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>Ladder diagram (if partial)
Consisting of 3 contactors
1. star, 2.delta,3.main</td><td>(3)</td><td></td><td></td></tr>
<tr><td></td><td></td><td>Complete ladder diagram Without Inter locking for star and delta contactors</td><td>(5)</td><td>7</td><td>15</td></tr>
</table>