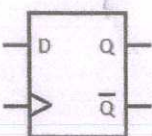
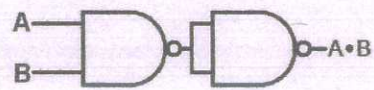


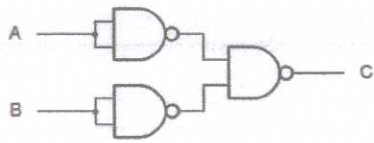
Scheme of valuation (Scoring indicators)

REVISION: 2015

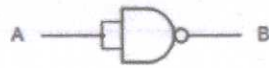
COURSE CODE: 4032

COURSE TITLE: DIGITAL ELECTRONICS AND MICROPROCESSOR

Qst No:	SCORING INDICATOR	Split Up Score	Sub Total	total																				
PART A																								
I																								
1.	Binary, Octal and Hexadecimal number systems.	2																						
2.	0101011	2																						
3.	D Flip-flop <div style="display: flex; align-items: center;"> <div style="margin-right: 20px;"> <p>Symbol</p>  </div> <div> <p>Table of truth:</p> <table border="1" style="border-collapse: collapse; text-align: center;"> <thead> <tr> <th>clk</th> <th>D</th> <th>Q</th> <th>\bar{Q}</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Q</td> <td>\bar{Q}</td> </tr> <tr> <td>0</td> <td>1</td> <td>Q</td> <td>\bar{Q}</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table> </div> </div>	clk	D	Q	\bar{Q}	0	0	Q	\bar{Q}	0	1	Q	\bar{Q}	1	0	0	1	1	1	1	0	2		10
clk	D	Q	\bar{Q}																					
0	0	Q	\bar{Q}																					
0	1	Q	\bar{Q}																					
1	0	0	1																					
1	1	1	0																					
4.		2																						
5.	The number of states of a counter is called its modulus. Accumulator, PC, SP, Flag register.	2																						
PART B																								
II																								
1.	Basic gates with NAND gates. AND gate 	2																						
		2																						
		2	6																					



OR Gate



NOT Gate

2.

6

6

3.

6

6

Applications of flip-flop

Counters

Frequency dividers

Registers

Comparators

Timing signal generation

Data transfer

Mono stable multi vibrator

4.

Serial decoding

4x1 Multiplexer

3

3

6

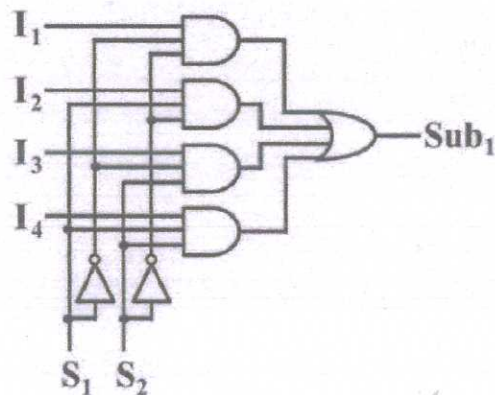


Diagram 3 marks ;

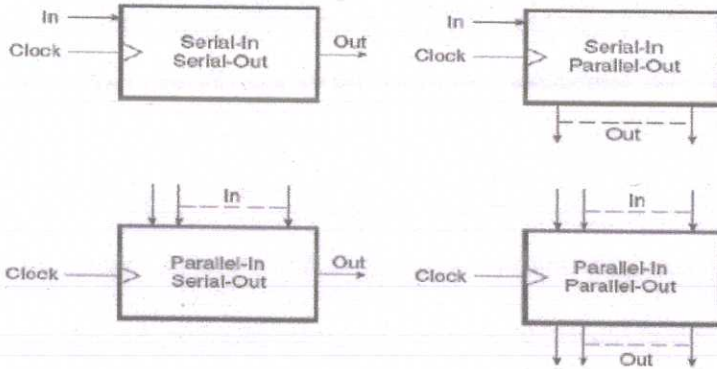
5.

SISO- Serial In Serial Out Shift register

SIPO-Serial In Parallel Out Shift register

PISO-Parallel In Serial Out Shift register

PIPO-Parallel In Parallel Out Shift register



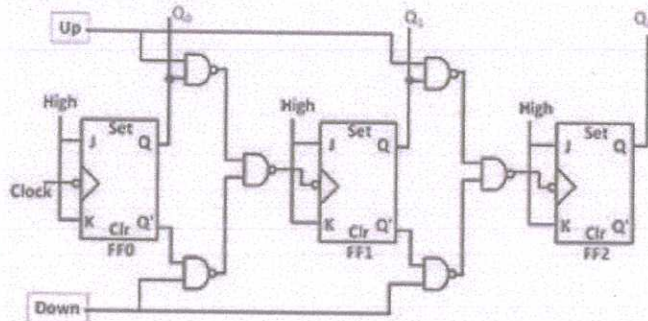
3

6

3

6.

UP-DOWN Counter

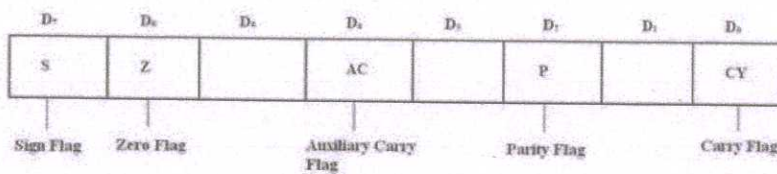


6

6

7.

Flag register of 8085 microprocessor



4

6

42

2

Diagram 4 marks

Explanation of flags 2 marks

PART C

III

65535

268.625

a

HEX: F F F F

1 0 C . A

BINARY: 1111 1111 1111 1111

0001 0000 1100 . 1010

2

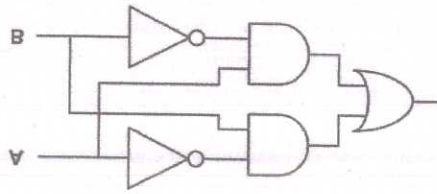
2

2

2

8

b XOR



A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

Logic circuit 3 marks

Truth table 2 marks

Explanation 2 marks

3
2
2

7

15

IV

a

$$\begin{array}{r}
 1011 \\
 X \quad 1101 \\
 \hline
 1011 \\
 0000 \\
 1011 \\
 1011 \\
 \hline
 10001111
 \end{array}$$

$11101 \div 1100 = 10.01101$

4

4

8

b

Comparison of TTL and CMOS logic family

	TTL	ECL	CMOS
Base Gate	NAND	OR/NOR	NAND/NOR
Fan-in	12-14	>10	>10
Fan-out	10	25	50
Power dissipation (mW)	10	175	0.001
Noise Margin	0.5V	0.16V (lowest)	1.5V (Highest)
Propagation Delay (ns)	10	<3 lowest	15 Highest
Noise immunity	Very good	good	excellent

7

7

15

V

UNIT II

a

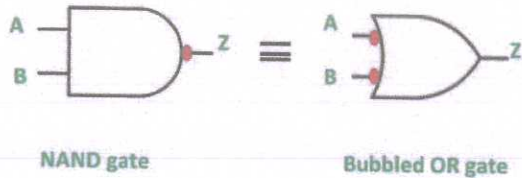
De Morgan's theorems

1. The compliment of sum is equal to the product of its compliments.

$$A+B = A.B$$

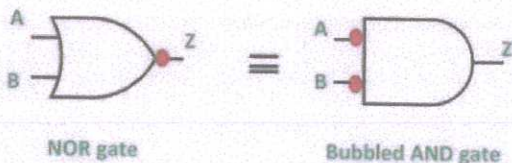
2. The compliment of a product is equal to sum of its compliments.

$$A.B = A+B$$



NAND gate

Bubbled OR gate



NOR gate

Bubbled AND gate

Theorems 4 marks

Gate diagram 2 marks

Truth tables 2 marks

Half adder

b

Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (S) and carry bit (C) as the output. If A and B are the input bits, then sum bit (S) is the X-OR of A and B and the carry bit (C) will be the AND of A and B. From this it is clear that a half adder circuit can be easily constructed using one X-OR gate and one AND gate. Half adder is the simplest of all adder circuit, but it has a major disadvantage. The half adder can add only two input bits (A and B) and has nothing to do with the carry if there is any in the input. So if the input to a half adder have a carry, then it will be neglected it and adds only the A and B bits. That means the binary addition process is not complete and that's why it is called a half adder. The truth table, schematic representation and XOR//AND realization of a half adder are shown in the figure below.

Explanation 3 marks

Diagram 2 marks

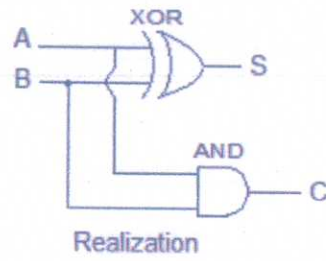
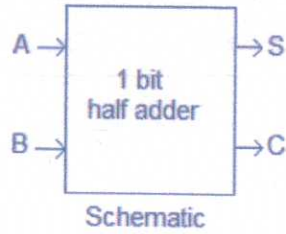
Truth table 2 marks

4	8	15
2		
2		

3

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

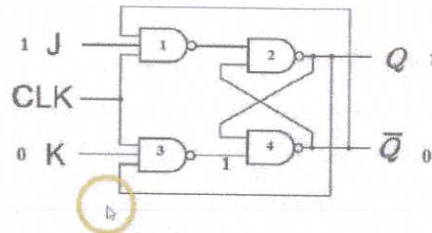
Truth table



2
2
7

VI
a

J-K Flip-flop



NAND gate

A	B	C	Z
1	1	1	0
1	1	0	1
1	0	1	1
1	0	0	1
0	1	1	1
0	1	0	1
0	0	1	1
0	0	0	1

Screencast-O-Matic.com

J	K	CLK	Q	Q̄	Comment
0	0	↑	Q	Q̄	Latch
1	0	↑	1	0	SET
0	1	↑	0	1	RESET
1	1	↑	Q̄	Q	TOGGLE
X	X	Any Thing Else	Q	Q̄	NO Change!

4
2
2
8

Logic circuit 4 marks

Truth table 2 marks

Explanation 2 marks

b

$$Y = \bar{A} \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot B \cdot \bar{C} + A \cdot \bar{B} \cdot \bar{C} + A \cdot B \cdot \bar{C}$$

$$Y = (\bar{A} \cdot \bar{B} + \bar{A} \cdot B + A \cdot \bar{B} + A \cdot B) \bar{C}$$

$$Y = (\bar{A}(\bar{B} + B) + A(\bar{B} + B)) \bar{C}$$

$$Y = (\bar{A}(1) + A(1)) \bar{C}$$

$$Y = (\bar{A} + A) \bar{C}$$

$$Y = \bar{C}$$

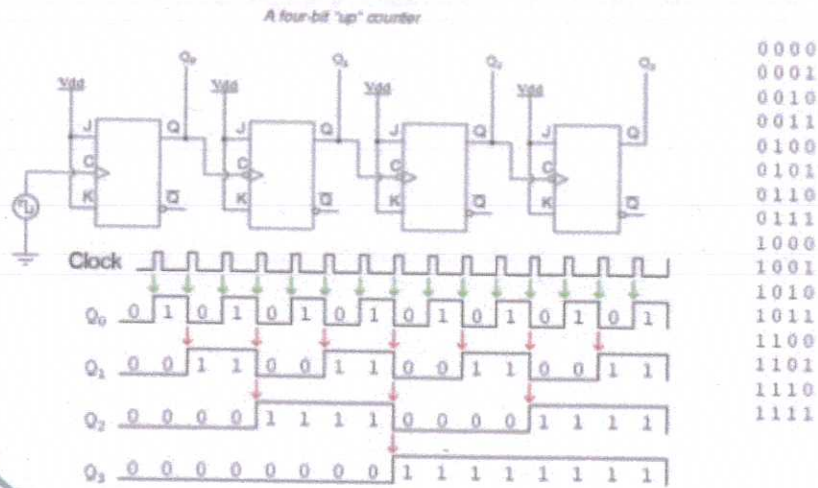
7
7
15

VII

MOD-16 RIPPLE COUNTER

MOD 16 Asynchronous Up counter – (Negative Triggered)

Figure 2.5 : MOD 16 Asynchronous Up Counter



DEE2034 : DIGITAL ELECTRONICS

14

Logic diagram 5 marks

Wave form 4 marks

Truth table 3 marks

Explanation 3 marks

VIII

a

R -2 R ladder DAC

- R-2R weighted resistor ladder network uses only 2 set of resistors- R and 2R. If you want to build a very precise DAC, be precise while choosing the values of resistors that will exactly match the R-2R ratio.
- This is a 4 bit DAC. Let us consider the digital data $D_3D_2D_1D_0 = 0001$ is applied to the DAC, then the Thevenin equivalent circuit reduction is sV_{ref} is nothing but the input binary value reference voltage, that is for binary 1, $V_{ref} = 5V$ and for binary 0, $V_{ref} = 0V$.
- For 0001 only $D_0 = V_{ref}$, all other inputs are at 0V and can be treated as ground. So finally $V_{ref}/16$ volt is appearing as the input to op amp. This value gets multiplied by the gain of op amp circuit - (R_f/R_i) .
- If we proceed in this manner (Thevenin equivalent reduction), we will get

$$V_{out} = -\frac{R_f}{R_i} V_{ref} \left[\frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2} \right]$$

- Note that you can build a DAC with any number of bits you want, by simply enlarging the resistor network, by adding more R-2R resistor branches.

5

15

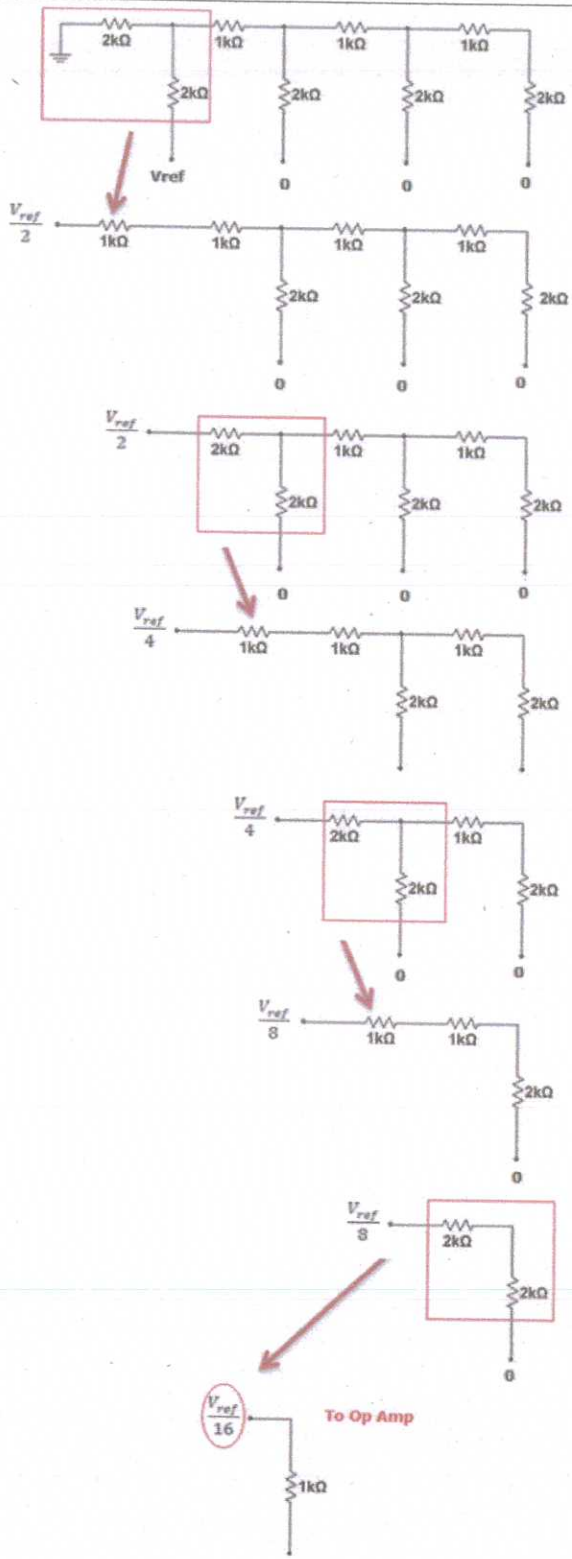
15

4

3

3

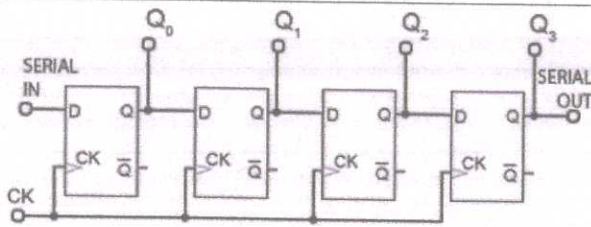
4



4 8

Figures 4 marks
 Explanation 4 marks

SISO Register



UNIT IV

IX

Features of 8085 microprocessor

It is an 8 bit microprocessor (each character is represented by 8 bits or a byte).

It is manufactured with N-MOS (n-type Metal Oxide Semiconductor) technology implemented with 6200 transistors.

It has 16-bit address lines - A0-A15 (to point the memory locations) and hence can point up to $2^{16} = 65535$ bytes (64KB) memory locations.

The first 8 lines of address bus and 8 lines of data bus are multiplexed AD0-AD7. Data bus is a group of 8 lines D0-D7.

It provides 5 level interrupts and supports external interrupt request.

A 16 bit program counters (PC).

A 16 bit stack pointer (SP).

It provides 1 accumulator, 2 flag register, six 8-bit general purpose register arranged in pairs: BC, DE, HL and 2 special purpose registers.

It consists of 74 instruction sets.

It performs arithmetic and logical operations.

It provides status for advanced control signals, On chip clock generator.

It requires a signal +5V power supply and operates at 3.2 MHZ single phase clock with maximum clock frequency 6 MHz and minimum clock frequency 500 kHz.

Serial input/output por

Addressing Modes of 8085 microprocessor

7

7

15

7

7

2

X	<p>These are the instructions used to transfer the data from one register to another register, from the memory to the register, and from the register to the memory without any alteration in the content. Addressing modes in 8085 is classified into 5 groups –</p> <p>Immediate addressing mode</p> <p>In this mode, the 8/16-bit data is specified in the instruction itself as one of its operand. For example: MVI K, 20F: means 20F is copied into register K.</p> <p>Register addressing mode</p> <p>In this mode, the data is copied from one register to another. For example: MOV K, B: means data in register B is copied to register K.</p> <p>Direct addressing mode</p>	2 2 2	8	15
	<p>In this mode, the data is directly copied from the given address to the register. For example: LDB 5000K: means the data at address 5000K is copied to register B.</p> <p>Indirect addressing mode</p> <p>In this mode, the data is transferred from one register to another by using the address pointed by the register. For example: MOV K, B: means data is transferred from the memory address pointed by the register to the register K.</p> <p>Implied addressing mode</p> <p>This mode doesn't require any operand; the data is specified by the opcode itself. For example: .</p> <p>Architecture</p> <p>8085 Microprocessor – Functional Units</p> <p>8085 consists of the following functional units –</p> <p>Accumulator</p> <p>It is an 8-bit register used to perform arithmetic, logical, I/O & LOAD/STORE operations. It is connected to internal data bus & ALU.</p> <p>Arithmetic and logic unit</p> <p>As the name suggests, it performs arithmetic and logical operations like Addition, Subtraction, AND, OR, etc. on 8-bit data.</p> <p>General purpose register</p> <p>There are 6 general purpose registers in 8085 processor, i.e. B, C, D, E, H & L. Each register can hold 8-bit data.</p> <p>These registers can work in pair to hold 16-bit data and their pairing combination is like B-C, D-E & H-L.</p> <p>Program counter</p> <p>It is a 16-bit register used to store the memory address location of the next instruction to be executed. Microprocessor increments the program whenever an instruction is being executed, so that the program counter points to the memory address of the next instruction that is going to be executed.</p> <p>Stack pointer</p>			

It is also a 16-bit register works like stack, which is always incremented/decremented by 2 during push & pop operations.

Temporary register

It is an 8-bit register, which holds the temporary data of arithmetic and logical operations.

Flag register

It is an 8-bit register having five 1-bit flip-flops, which holds either 0 or 1 depending upon the result stored in the accumulator.

These are the set of 5 flip-flops –

- Sign (S)
- Zero (Z)
- Auxiliary Carry (AC)
- Parity (P)
- Carry (C)

Instruction register and decoder

It is an 8-bit register. When an instruction is fetched from memory then it is stored in the Instruction register. Instruction decoder decodes the information present in the Instruction register.

Timing and control unit

It provides timing and control signal to the microprocessor to perform operations. Following are the timing and control signals, which control external and internal circuits –

- Control Signals: READY, RD', WR', ALE
- Status Signals: S0, S1, IO/M'
- DMA Signals: HOLD, HLDA
- RESET Signals: RESET IN, RESET OUT

Interrupt control

As the name suggests it controls the interrupts during a process. When a microprocessor is executing a main program and whenever an interrupt occurs, the microprocessor shifts the control from the main program to process the incoming request. After the request is completed, the control goes back to the main program.

There are 5 interrupt signals in 8085 microprocessor: INTR, RST 7.5, RST 6.5, RST 5.5, TRAP.

Serial Input/output control

It controls the serial data communication by using these two instructions: SID (Serial input data) and SOD (Serial output data).

Address buffer and address-data buffer

The content stored in the stack pointer and program counter is loaded into the address buffer and address-data buffer to communicate with the CPU. The memory and I/O chips are connected to these buses; the CPU can exchange

the desired data with the memory and I/O chips.

Address bus and data bus

Data bus carries the data to be stored. It is bidirectional, whereas address bus carries the location to where it should be stored and it is unidirectional. It is used to transfer the data & Address I/O devices.

8085 Architecture

We have tried to depict the architecture of 8085 with this following image -

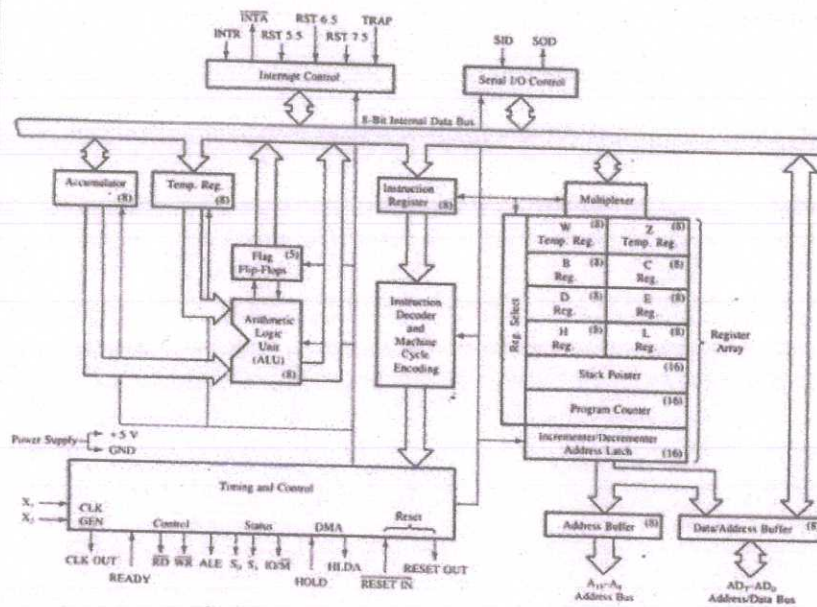


Diagram 8 marks

Explanation 7 marks

8

15

15